Commodore

A 2088

PC Emulator Card
Service Manual

1/89

Commodore

PC Emulator-Card
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A2088 SPECIFICATIONS

Card Type:	Uses both Amiga bus (100 pin) and IBM-PC/XT bus system of the Amiga A2000 (goes into combined position).
Function:	Provides an 8088 co-processor system with IBM-PC/XT compatibility. Uses AutoConfig features of the Amiga. Socket for 8087 math co-processor.

DATA - 8088 SIDE

Clock Speed:	4.77 MHz
Memory:	512 kByte RAM
ROM:	16 kByte BIOS
Interfaces:	1 internal floppy disk drive 5.25" 360 Kbyte capacity 1 external floppy disk drive 5.25" 360 Kbyte capacity or 3.5" 720 Kbyte capacity (Amiga 1020 / 1010) Parallel Port (Centronics, IBM-PC compatible emulated on Amiga parallel port).
Slots:	3 IBM-PC compatible full size slots
Keyboard:	IBM-PC/XT keyboard emulated on the Amiga keyboard
Video Display:	IBM-PC monochrome text mode and color mode are emulated in seperat AmigaDOS windows simultaneously.
System Software:	MS-DOS

DATA - AMIGA SIDE

Inter-System Communication:	64 kByte dual-port RAM as inter-process buffer 64 kByte dual-port scratch memory on Amiga side Interrupt logic Janus emulation software

BUS INTERFACE

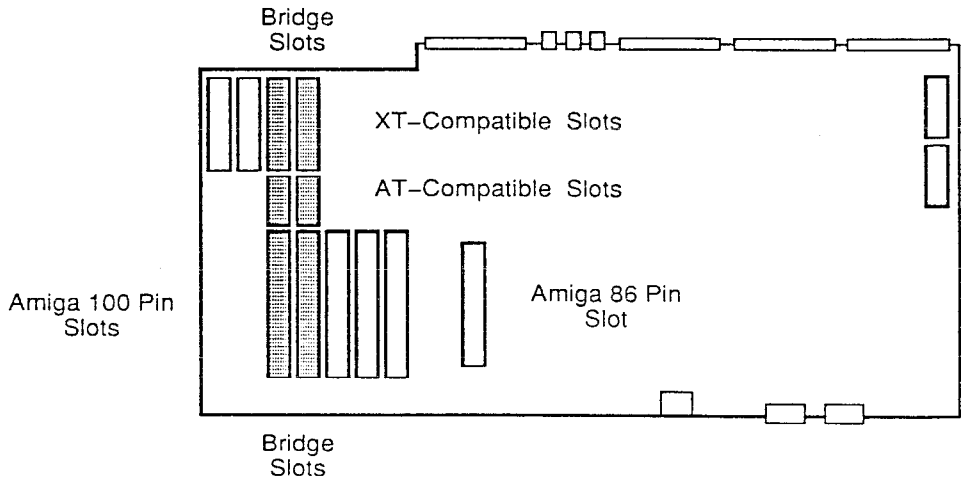
Type:	Fast dual-port memory, full speed CPU access during system DMA
Card Size:	Full size Amiga 2000 card
Power:	Supplied by system
Included Items:	Janus emulation software on 3.5" floppy disk Internal floppy disk drive 5.25" 360 Kbyte capacity

Installing the Bridgeboard Hardware

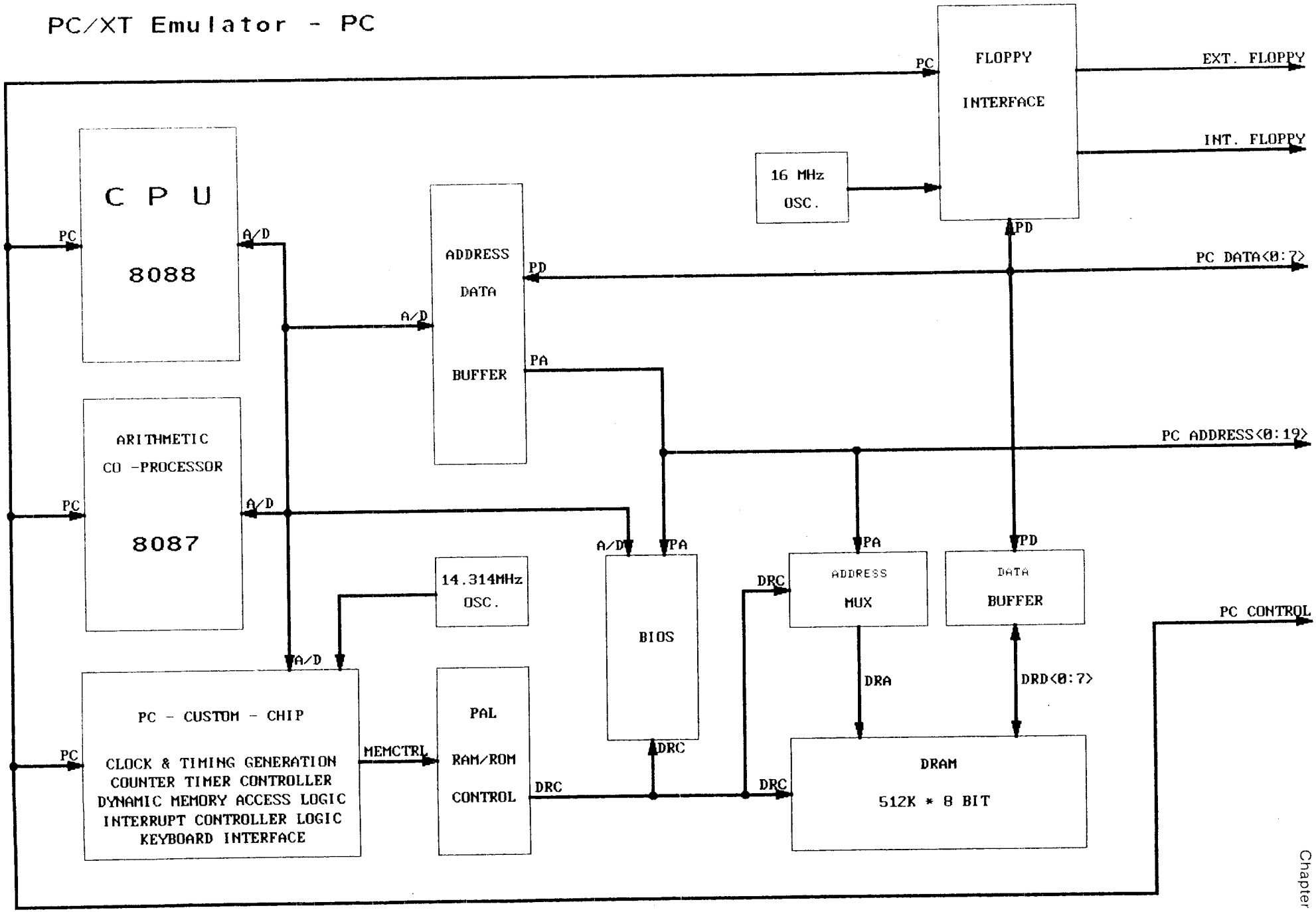
Before you install the Bridgeboard in your A2000, **TURN OF ALL POWER.** It may make it physically easier to install the Bridgeboard if you disconnect some or all of the equipment connected to the A2000. Before you try to operate the unit, be sure to read *all* the installation and setup instructions in the Bridgeboard users guide, and reconnect any equipment you may have disconnect.

Where the Bridgeboard Goes:

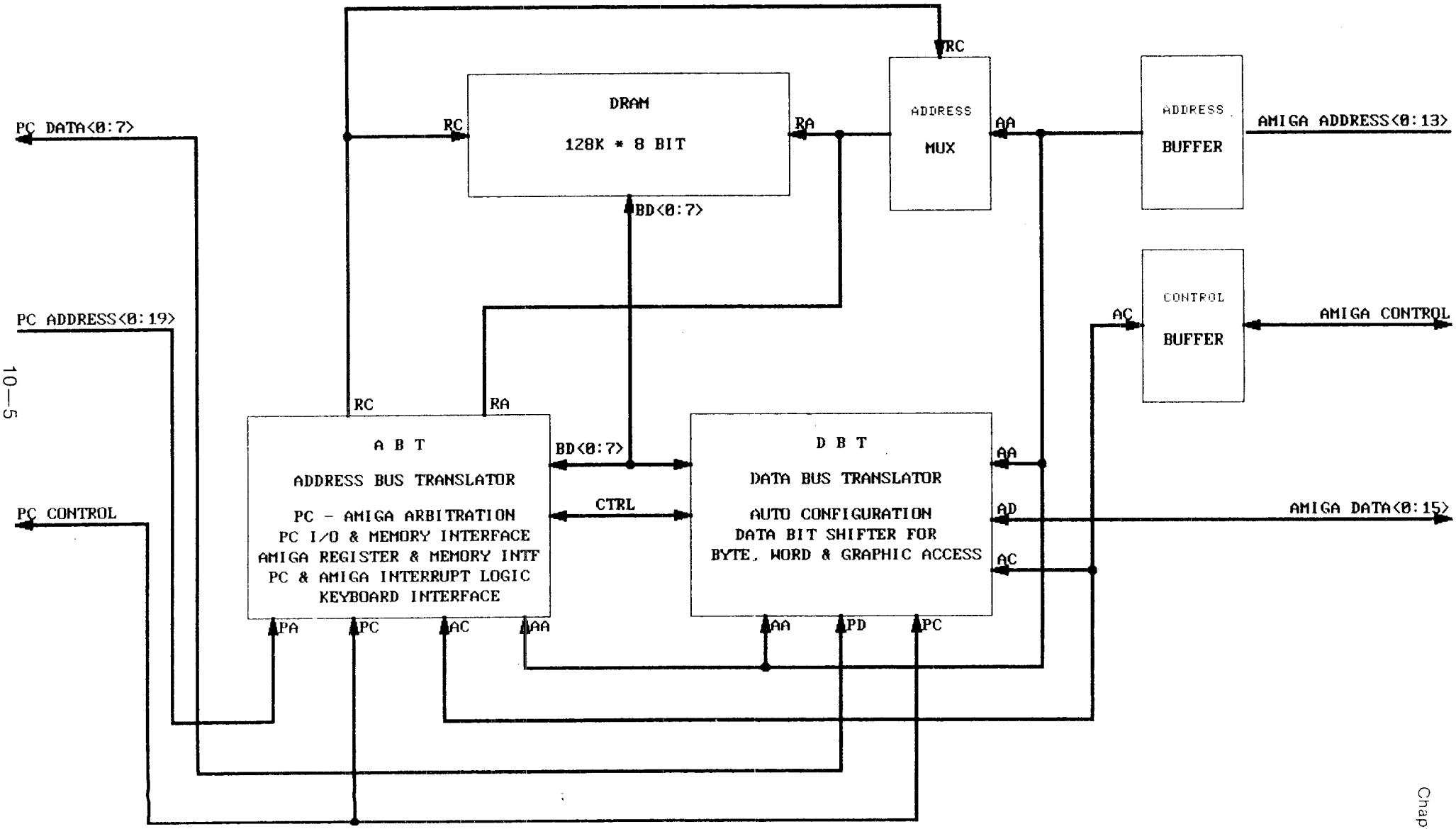
The Bridgeboard plugs into the internal expansion slot area located at the left of the A2000.
There are five slots on the Amiga system bus and four slots on a secondary bus that is IBM PC/XT–compatible. Two pairs of slots (a pair being one slot on the Amiga bus and one slot on the IBM bus) are physically situated to allow the Bridgeboard to be inserted.



PC/XT Emulator - PC

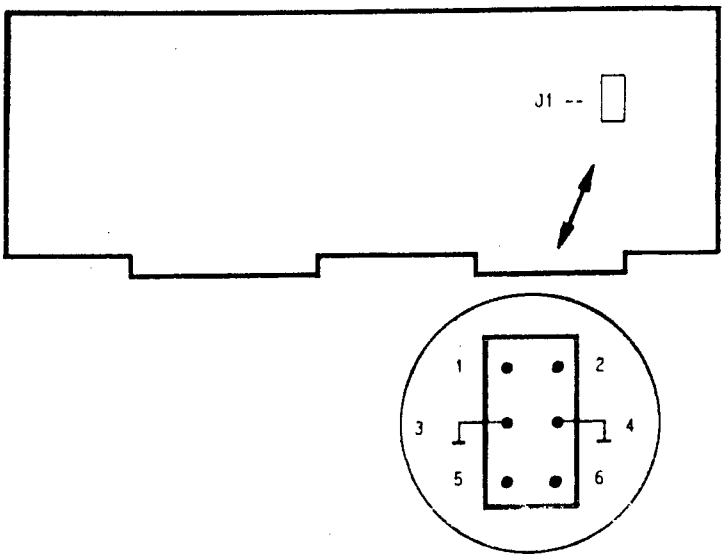


PC/XT Emulator - interface



VIDEO STARTUP TABLE PC – EMULATOR

Location of J1 Jumper on Bridgeboard:



J1 Default display jumper pair located near the rear center of the Bridgeboard. (Two sets of three pins)

Startup-Mode	*Jumper Setting*
Monochrome (default)	
Color 40 x 25	
Color 80 x 25	
None	

DASH NO	01	ITEM	PART-NUMBER	DESCRIPTION	REF DES	NOTES
		01				
	REF	02	380 756 - 01	SCHEMATIC		
	REF	03	380 757 - 01	PCB ARTWORK		
	1	04	380 758 - 01	FABRICATION		
		05				
	1	06	380 658 - 01	IC, ADDRESS BUS TRANSL.	U 40	
	1	07	380 659 - 01	IC, DATA BUS TRANSL. 5718	U 41	
		08				
		09				
		10				
	1	11	380 200 - 01	IC, 8088	U 1	
	-	12	380 201 - 01	IC, 8087	U 2	OPTIONAL
		13				
		14				
	1	15	380 783 - 01	IC, PAL RAM DECODER, EMULATOR	U 29	PROD OF 16L8;P/N:380219-01
	1	16	380 784 - 01	IC, PAL I/O DECODER	U 50	PROD OF 16L8;P/N:380219-01
	-	17	380 785 - 01	IC, PAL CONFIGURATION	U 39	ONLY USED IF JUMPER JA1 OPEN
		18				
	1	19	380 786 - 01	IC, FE 2010	U 7	VENDOR:FARADAY
		20				
		21				
	8	22	380 223 - 01	IC, DRAM 256K X 1, 150 nS	U12-27	
	4	23	380 256 - 01	IC, DRAM 64K X 4, 150 nS	U 32-35	
		24				
		25				
	1	26	380 787 - 01	IC, FDC 9268	U 42	VENDOR:SMC
		27				
	1	28	380 788 - 01	IC, BIOS PC-EMULATOR	U 28	PROD OF 27128EPROM OR ROM 23128 TAC = 250 NS
		29				
		30				
		31				
	2	32	380 227 - 04	IC, 74 HCT 158	U 10,11	
	2	33	380 227 - 58	IC, 74 HCT 257	U 36,37	
		34				
	2	35	901 522 - 06	IC, 7406	U 43,44	
		36				
		37				

DASH NO.	01	ITEM	PART-NUMBER	DESCRIPTION	REF DES	NOTES
		38				
	1	39	901 521 - 03	IC, 74 LS 08	U 45	
	1	40	901 521 - 30	IC, 74 LS 14	U 46	
	1	41	901 521 - 20	IC, 74 LS 125	U 47	
	1	42	901 521 - 15	IC, 74 LS 133	U 38	
	1	43	901 521 - 28	IC, 74 LS 164	U 48	
	1	44	901 521 - 34	IC, 74 LS 175	U 49	
	2	45	901 521 - 13	IC, 74 LS 244	U 8,9	
	3	46	901 521 - 46	IC, 74 LS 245	U 3,30,51	
	3	47	901 521 - 29	IC, 74 LS 373	U 4-6	
		48				
		49				
		50				
	1	51	324 667 - 01	DIGITAL DELAY LINE	U 31	
		52				
		53				
	1	54	325 566 - 10	OSCILLATOR 16 MHZ, HYBRID	OSC 1	+/- 5% +/- 50 PPM
		55				VENDOR: KINSEKI
	1	56	900 558 - 01	QUARZ 14.31818 MHZ	QU 1	HC-18U
		57				
	1	58	251 070 - 18	CAP CER RADIAL 47 PF	C 52	+/- 5% SP:5 MM
	10	59	251 070 - 22	CAP CER RADIAL 100 PF	C 55,61,62	C63-69 +/- 5% SP:5 MM
	2	60	251 071 - 30	CAP CER RADIAL 470 PF/50V	C 71,72	+/-10% SP:5 MM
		61				
		62				
		63				
	20	64	900 020 - 01	CAP CER RADIAL 0.1 UF	C 3-6,8-11	C30,36-38,43-49,51
		65				+/- 20%, SP:5 MM
		66				
	32	67	900 022 - 01	CAP CER RADIAL 0.22 UF/50V	C 1,2,7	C12-29,31-35,39-42,50
		68			C53,54,60,70	+/- 10%, SP:5 MM
		69				
		74				
		71				
	4	72	900 100 - 27	CAP ELECTR. AXIAL 47UF/25V	C 56-59	
		73				
		74				

DASH NO.	01	ITEM	PART-NUMBER	DESCRIPTION	REF DES	NOTES
	1	75	324 219 - 01	TRANSISTOR BC-327 B	T 1	
		76				
		77				
	1	78	902 417 - 03	RES PACK 4 X 1K	RN 9	SINGLE LINE 5 PIN,SP:2.54 MM
	1	79	902 410 - 08	RES PACK 9 X 4K7	RN 10	SINGLE LINE 10 PIN,SP:2.54 MM
		80				
		81				
	3	82	902 412 - 05	RES PACK 8 X 4K7	RN 1,2,11	SINGLE LINE 9 PIN,SP:2.54 MM
		83				
		84				
	6	85	902 422 - 07	RES PACK 4 X 68 OHM	RN 3-8	SINGLE LINE 8 PIN,SP:2.54 MM
		86				
		87				
	2	88	901 550 -105	RESISTOR CARBON 33 OHM .25W 5%	R 7,8	
	2	89	901 550 - 49	RESISTOR CARBON 100 OHM .25W 5%	R 3,5	
		90				
	3	91	901 550 - 01	RESISTOR CARBON 1 K .25W 5%	R 1,10,11	
	1	92	901 550 - 18	RESISTOR CARBON 2K2 .25W 5%	R 6	
	2	93	901 550 - 19	RESISTOR CARBON 4K7 .25W 5%	R 2,9	
		94				
	1	95	901 550 - 84	RESISTOR CARBON 1M .25W 5%	R 4	
		96				
		97				
		98				
	2	99	380 333 - 01	JUMPER RM: 2.54 MM		
	2	100	903 781 - 01	WIRE JUMPER	JA 1,2	
		101				
		102				
	1	103	903 345 - 03	HEADER ASSY DUAL ROW .100CTR.	J 1	6 PIN
		104				
	1	105	903 345 - 17	HEADER ASSY DUAL ROW .100CTR.	J 3	34 PIN REMOVE PIN 3 AT ASSEMBLY
	1	106	327 033 - 01	CONNECTOR 23 PIN SUB MINI "D" FEMALE	J 4	
	S	105	310 975 - 01	CONNECTOR 23 PIN SUB MINI "D" FEMALE	J 4	SUB FOR ITEM 106
	1	108	903 326 - 02	HEADER ASSY SINGLE ROW .100 CTR.	J 2	2 PIN
	1	109	903 326 - 08	HEADER ASSY SINGLE ROW .100 CTR.	J 7	8 PIN, REM.PIN 6 AT ASSEMBLY
		110				
	1	111	904 150 - 05	IC SOCKET 28 PIN	U 28	

DASH NO.	01	ITEM	PART-NUMBER	DESCRIPTION	REF DES	NOTES
	8	112	904 150 - 02	IC SOCKET 16 PIN	U 20-27	
	2	113	904 150 - 08	IC SOCKET 20 PIN	U 29,50	
	3	114	904 150 - 06	IC SOCKET 40 PIN	U 1,2,42	
	3	115	380 789 - 01	IC SOCKET 84 PIN	U 7,40,41	PLCC
	-	116	904 150 - 08	IC SOCKET 20 PIN	U 39	ONLY USED IF JA1 OPEN
	2	117	906 800 - 03	SCREW, PAN HEAD M 3 X 8		
	2	118	905 652 - 04	LOCKWASHER EXT. TOOTH. Ø 3.2 MM		
	2	119	905 960 - 03	NUT HEX M 3		
		120				
	2	121		RIVET DOME		SUB. FOR ITEM 117-119
		122				
	1	123	380 120 - 08	EXTENSION CARD PANEL		
		124				
		125				

PART NO.	DESCRIPTION
380 755 - 01	PCB ASSY PC/XT EMULATOR 512 KB

REVISIONS

LTR	ZONE	DESCRIPTION	DATE	APPROVED
1		ENGINEERING RELEASE	01-21-87	
2		UPDATE		
3				
4				
5				
6				
7		UPDATE		
8		PILOT PRODUCTION RELEASE	10-06-87	
A		REVISED PER ECO 870241	1-11-88	
B		REVISED PER ECO 870458	2-22-88	
C		REVISED PER ECO 870392	5-10-88	

1. SHEET OF SIZE

ASSY DWG

NOTES:

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commodore	TITLE: PCB ASSY PC/XT EMULATOR 512 KB	DRAWN BY: GL	DATE 10-6-87	ENGR:	10-6-87	SIZE B	DRAWING NUMBER 380 755
		CHKD.		APPR:			SHEET 1 OF 6

1715 Gebr. Wichmann

QUANTITY REQD PER PART / DASH NO.	ITEM	DS	PART NUMBER	DESCRIPTION	REF DES	BEND	NOTES
	01						
REF	02		380 756 - 01	SCHEMATIC			
REF	03		380 757 - 01	PCB ARTWORK			REV.3
1	04		380 758 - 01	FABRICATION			
	05						
1	06		380 658 - 01	IC, ADDRESS BUS TRANSL.	U 40		
1	07		380 659 - 01	IC, DATA BUS TRANSL. 5718	U 41		
	08						
	09						
	10						
1	11		380 200 - 01	IC, 8088	U 1		
-	12		380 201 - 01	IC, 8087	U 2		OPTIONAL
	13						
	14						
1	15		380 783 - 01	IC, PAL RAM DECODER EMULATOR	U 29		PROD OF P/N:390071-02 16L8A
1	16		380 784 - 01	IC, PAL I/O DECODER	U 50		PROD OF P/N:390071-02 16L8A
	17						
	18						
1	19		380 786 - 01	IC, FE 2010	U 7		VENDOR:FARADAY
	20						
	21						
16	22		380 223 - 01	IC, DRAM 256K X 1, 150 nS	U12-27		
4	23		390 083 - 02	IC, DRAM 64K X 4, 150 nS	U 32-35		
	24						
	25						
1	26		312710-01	IC, FDC 9268	U 42		VENDOR:SMC
	27						
1	28		380 788 - 04	IC, BIOS PC-EMULATOR	U 28		PROD OF 27128EPROM OR ROM 23128
	29						TAC = 250 NS
	30						
	31						
2	32		380 227 - 04	IC, 74 HCT 158	U 10,11		
2	33		380 227 - 58	IC, 74 HCT 257	U 36,37		
	34						
2	35		901 522 - 06	IC, 7406	U 43,44		
1	36		901 525 - 04	IC, 74 S 00	U 39		
S	37		390 092 - 02	IC, 74 F 00	U 39		SUBST. FOR ITEM 36

commodore

TITLE: PCB ASSY PC/XT EMULATOR 512KB

DRWN BY:	DATE	ENGR:	DATE	SIZE		REV	SHT
CHKD:	10-6-87	APPR:	12-2-87	B	380 755	C	2/6

QUANTITY REQD PER PART / DASH NO.	ITEM	DS	PART NUMBER	DESCRIPTION	REF DES	BEND	NOTES
	38						
1	39		901 521 - 03	IC, 74 LS 08	U 45		
1	40		901 521 - 30	IC, 74 LS 14	U 46		
1	41		901 521 - 20	IC, 74 LS 125	U 47		
1	42		901 521 - 15	IC, 74 LS 133	U 38		
1	43		901 521 - 28	IC, 74 LS 164	U 48		
1	44		901 521 - 34	IC, 74 LS 175	U 49		
2	45		901 521 - 13	IC, 74 LS 244	U 8,9		
3	46		901 521 - 46	IC, 74 LS 245	U 3,30,51		
3	47		901 521 - 29	IC, 74 LS 373	U 4-6		
	48						
	49						
	50						
1	51		324 667 - 01	DIGITAL DELAY LINE	U 31		
	52						
	53						
1	54		325 566 - 10	OSCILLATOR 16 MHZ, HYBRID	OSC 1		+/- 5% +/- 50 PPM
	55						VENDOR: KINSEKI
1	56		900 558 - 01	QUARZ 14.31818 MHZ	QU 1		HC-18U
	57						
1	58		251 070 - 18	CAP CER RADIAL 47 PF	C 52		+/- 5% SP:5 MM
10	59		251 070 - 22	CAP CER RADIAL 100 PF	C 55,61,62		C63-69 +/- 5% SP:5 MM
3	60		251 071 - 30	CAP CER RADIAL 470 PF/50V	C 71,72,C100		+/-10% SP:5 MM
	61						
	62						
	63						
20	64		900 020 - 01	CAP CER RADIAL 0.1 UF	C 3-6,8-11		C30,36-38,43-49,51
	65						+/- 20%, SP:5 MM
	66						
32	67		900 022 - 01	CAP CER RADIAL 0.22 UF/50V	C 1,2,7		C12-29,31-35,39-42,50
	68				C53,54,60,70		+/- 10%, SP:5 MM
	69						
	70						
	71						
4	72		900 100 - 27	CAP ELECTR. AXIAL 47UF/25V	C 56-59		
	73						
	74						

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TITLE: PCB ASSY PC/XT EMULATOR 512 KB

DRWN BY:	DATE	ENGR:	DATE	SIZE		REV	SHT
CHKD:	10-6-87	APPR:	10-7-87	B	380755	C	3/6

QUANTITY REQD PER PART / DASH NO.	ITEM	DS	PART NUMBER	DESCRIPTION	REF DES	BEND	NOTES
1	75		324 219 - 01	TRANSISTOR BC-327 B	T 1		
	76						
	77						
1	78		902 417 - 03	RES PACK 4 X 1K	RN 9		SINGLE LINE 5 PIN,SP:2.54 MM
1	79		902 410 - 08	RES PACK 9 X 4K7	RN 10		SINGLE LINE 10 PIN,SP:2.54 MM
	80						
	81						
3	82		902 412 - 05	RES PACK 8 X 4K7	RN 1,2,11		SINGLE LINE 9 PIN,SP:2.54 MM
	83						
	84						
6	85		902 422 - 07	RES PACK 4 X 68 OHM	RN 3-8		SINGLE LINE 8 PIN,SP:2.54 MM
	86						
	87						
2	88		901 550 -105	RESISTOR CARBON 33 OHM .25W 5%	R 7,8		
2	89		901 550 - 49	RESISTOR CARBON 100 OHM .25W 5%	R 3,5		
	90						
3	91		901 550 - 01	RESISTOR CARBON 1 K .25W 5%	R 1,10,11		
1	92		901 550 - 18	RESISTOR CARBON 2K2 .25W 5%	R 6		
2	93		901 550 - 19	RESISTOR CARBON 4K7 .25W 5%	R 2,9		
	94						
1	95		901 550 - 84	RESISTOR CARBON 1M .25W 5%	R 4		
	96						
	97						
	98						
2	99		320 333 - 01	JUMPER RM: 2.54 MM			
1	100		903 781 - 01	WIRE JUMPER	JA 2		
	101						
	102						
1	103		903 345 - 03	HEADER ASSY DUAL ROW .100CTR.	J 1		6 PIN
	104						
1	105		903 345 - 17	HEADER ASSY DUAL ROW .100CTR.	J 3		34 PIN REMOVE PIN 3 AT ASSEMBLY
1	106		327 033 - 01	CONNECTOR 23 PIN SUB MINI "D" FEMALE	J 4		
S	105		310 975 - 01	CONNECTOR 23 PIN SUB MINI "D" FEMALE	J 4		SUB FOR ITEM 106
1	108		903 326 - 02	HEADER ASSY SINGLE ROW .100 CTR.	J 2		2 PIN
1	109		903 326 - 08	HEADER ASSY SINGLE ROW .100 CTR.	J 7		8 PIN, REM.PIN 6 AT ASSEMBLY
	110						
1	111		904 150 - 05	IC SOCKET 28 PIN	U 28		

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TITLE: PCB ASSY PC/XT EMULATOR 512 KB

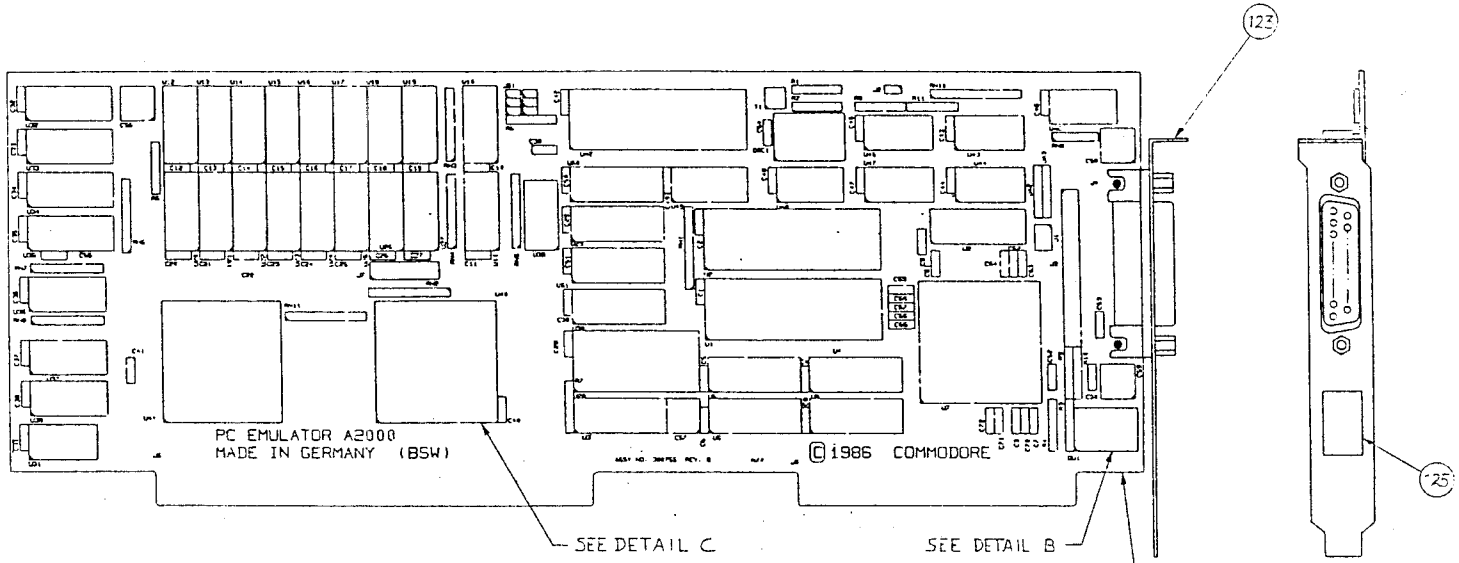
DRWN BY: GP. DATE 10-6-87 | CHKD: | ENGR: | APPR: | DATE 10-7-87

SIZE B | 380755 | REV C | SHT 4/6

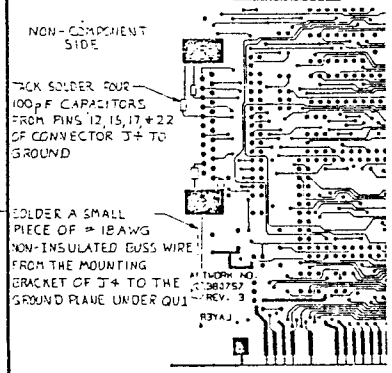
QUANTITY REQD PER PART / DASH NO.	ITEM	DS	PART NUMBER	DESCRIPTION	REF DES	BEND	NOTES
	112						
2	113		904 150 - 08	IC SOCKET 20 PIN	U 29,50		
3	114		904 150 - 06	IC SOCKET 40 PIN	U 1,2,42		
3	115		380 739 - 01	IC SOCKET 84 PIN	U 7,40,41		PLCC
	116						
2	117		906 800 - 03	SCREW, PAN HEAD M 3 X 8			
2	118		905 652 - 04	LOCKWASHER EXT. TOOTH. Ø 3.2 MM			
2	119		905 960 - 03	NUT HEX M 3			
	120						
2	121			RIVET DOME			SUB. FOR ITEM 117-119
	122						
1	123		380 120 - 08	EXTENSION CARD PANEL			
4	124		900462 - 37	CAPACITOR 100pF	C73 - C76		
1	125		316420 - 01	FCC LABEL A2088			AFFIX TO EXTENSION CARD PANEL
1	126		390260 - 01	BUSS WIRE			

commodore	TITLE: PCB ASSY PC/XT EMULATOR 512 KB	DRWN BY:	DATE 10-6-87	ENGR:	DATE 10-7-87	SIZE B	380755	REV	SHT 5/6
		CHKD:		APPR:					

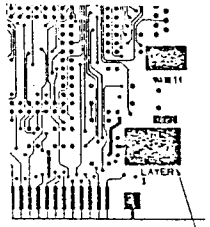
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



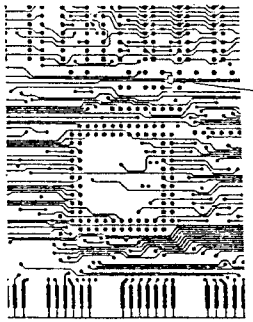
DETAIL A


NON-COMPONENT SIDE
TACK SOLDER FOUR 100pF CAPACITORS FROM PINS 12, 15, 17 & 22 OF CONNECTOR J4 TO GROUND
SOLDER A SMALL PIECE OF #18 AWG NON-INSULATED BUSS WIRE FROM THE MOUNTING BRACKET OF J4 TO THE GROUND PLANE UNDER QU1

DETAIL B



DETAIL C



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UNLESS OTHERWISE SPECIFIED
TOLERANCES ON DECIMALS
X .X ±.1 .XX ±.03 .XXX ±.005 ∠ ±1°
MATERIAL
FINISH

DRAWN BY: J HOOPER 5-4-88
CHKD
ENGR
APPR
USED ON A2088
NEXT ASSY

Commodore
1200 WILSON DRIVE
WEST CHESTER, PA 19380
(215) 431-9100

PCB ASSY, PC/XT EMULATOR 512 KB A2088

SIZE C | 380755 | REV C

SCALE ~ | SHEET 6 OF 6

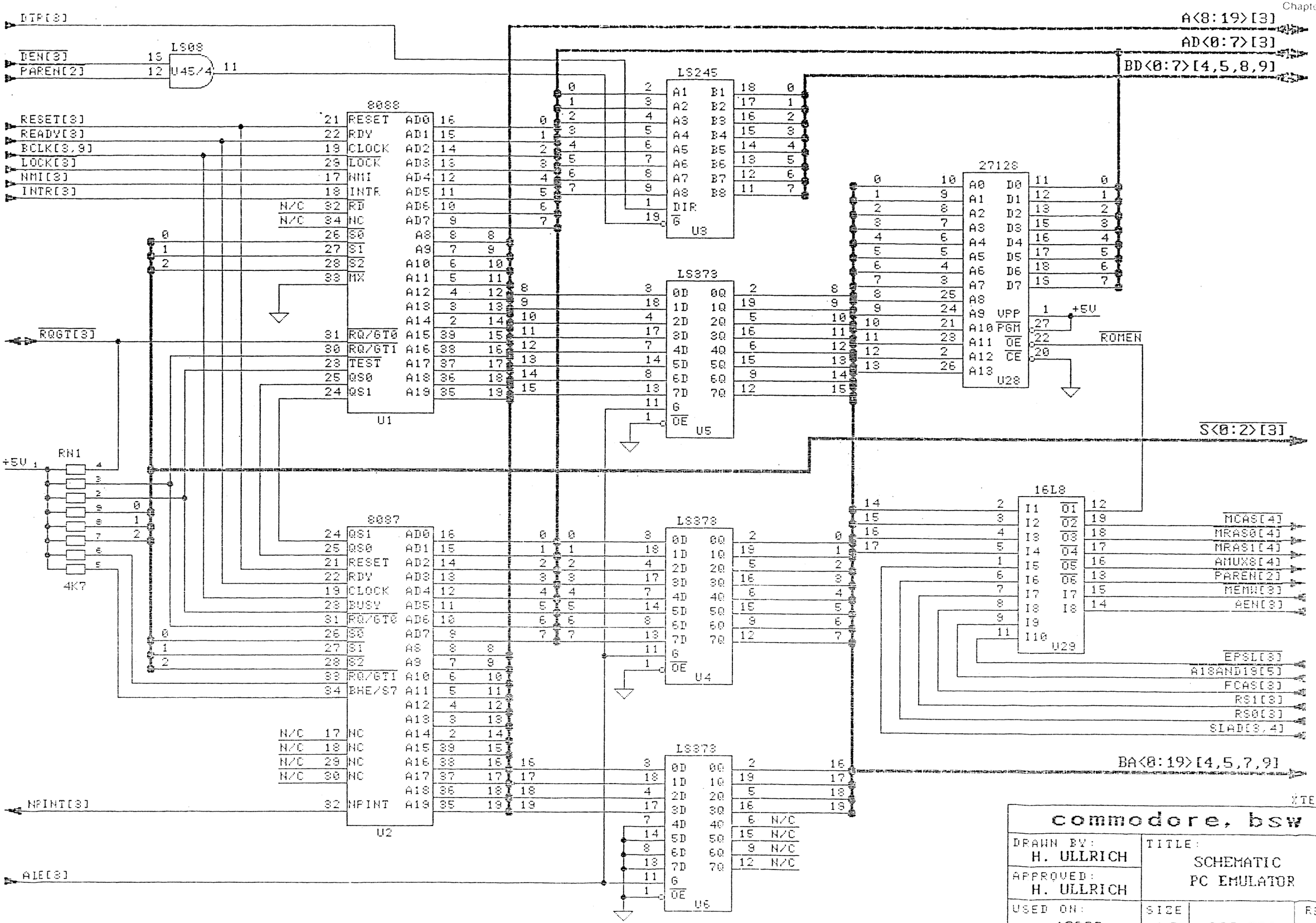
REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
1	ADVANCED ENGINEERING RELEASE	09-10-86	H. ULLRICH
2	UPDATE	10-13-86	"
3	UPDATE	11-06-86	"
4	UPDATE	11-13-86	"
5	PRODUCTION RELAESE	11-18-86	"
6	REWORKED PROD. RELEASE	05-20-87	"
A	REVISED PER ECO 870392	5-10-88	H. Ullrich

DRAWING FILES:	CONTENTS:
XTE_61.DWG	THIS SHEET
XTE_62.DWG	CPU SECTION
XTE_63.DWG	FE2010 SECTION
XTE_64.DWG	512KB MAIN RAM
XTE_65.DWG	FD CONTROLLER
XTE_66.DWG	128KB DUAL PORT RAM
XTE_67.DWG	ADDRESS BUS TRANSLATOR
XTE_68.DWG	DATA BUS TRANSLATOR
XTE_69.DWG	CONNECTORS
XTE_610.DWG	BLOCK CAPS

XTE_61

commodore, bsw			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC PC EMULATOR		
APPROVED: H. ULLRICH			
USED ON: A2000	SIZE A3	300 756	REV A



XTE_62

commodore, bsw			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC PC EMULATOR		
APPROVED: H. ULLRICH			
USED ON: A2088	SIZE A3	388 756	REV A

JUMPER	J1 SELECTS VIDEO STARTUP MODE:	JUMPER	1-3	3-5	2-4	4-6
		MON	-	X	-	X
		COL40	-	X	X	-
	- : OPEN, X : CLOSED	COL80	X	-	-	X
		NONE	X	-	X	-

A<8:19>[2]

AD<0:7>[2]

PWRGOOD[7]
IOCHCK[9]
KBCLK[7]
KBDATA[7]
IOCHRDY[7,9]

NPINT[2]
S<0:2>[2]
IRQ<2:7>[5,7,9]
DRQ<1:3>[5,9]

QU1 14.318MHZ
R3 100R
R4 1M
C52 47pF
R9 4K7
R10 1K
C72 470pF
C71 470pF
J1 N/C N/C N/C N/C

FE 2010

U7

VSS = 2,22,42,64
VDD = 1,43

X2 X1 AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 RESET_IN IOCK KBCLK KBDATA IORDY VID0 VID1 NPINT PTOUT PTIN A64K

A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 EPSL READY NMI RQGT DEN DTR ALE

IR02 IR03 IR04 IR05 IR06 IR07 DR01 DR02 DR03 S0 S1 S2 SPEAKER RS3 RS2 RS1 RS0 CAS RAMS SLAD

DACK0 DACK1 DACK2 DACK3 EOP OSC CLK RESET NC USCS AEN IORC IOWC MEMR MEMW BIOCS BALE INTR

N/C N/C N/C N/C N/C N/C

C61 C65 C68 C67 C66 C65 100pF
C64 C62 C63 100pF

EPSL[2]
READY[2]
NMI[2]
RQGT[2]
DEN[2]
DTR[2]
ALE[2]
RESET[2]

LS244 U8: A0 A1 A2 A3 A4 A5 A6 A7 → Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
BDACK<0:3>[5,7,9]
TC[5,9]
BOSC[7,9]
BCLK[2,9]
BRESET[5,9]

AEN[2]

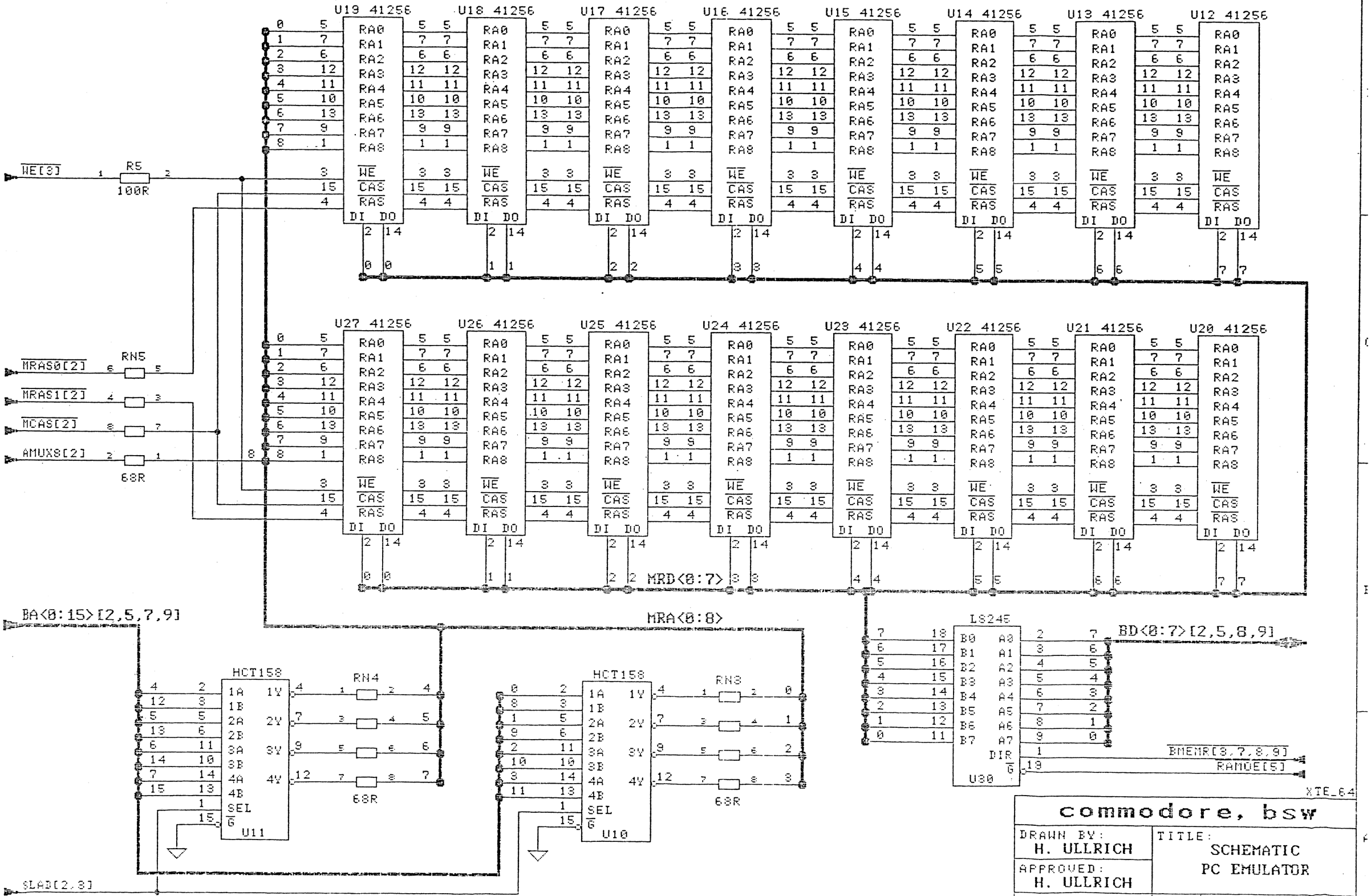
LS244 U9: A0 A1 A2 A3 A4 A5 A6 A7 → Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
BAEN[7,8,9]
BIORC[5,7,8,9]
BIOWC[5,7,9]
BMEMR[4,7,8,9]
BMEMW[7,9]
WE[4]
BALE[5,8]
BLOCK[7]

LOCK[2]
MEMW[2]
INTR[2]
SLAD[2,4]
RAMS[5]
RCAS[2]
RS0[2]
RS1[2]

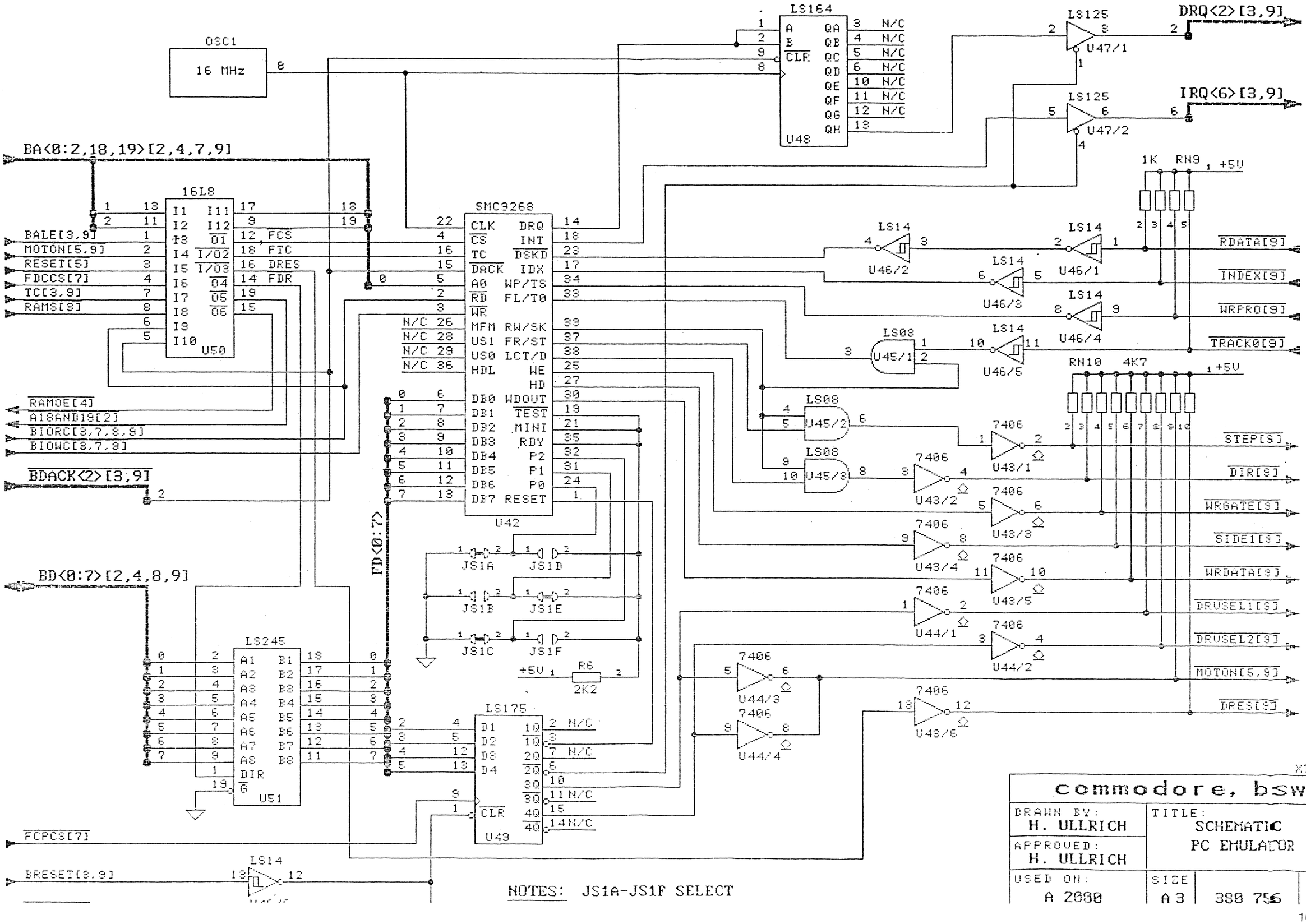
+5V
R1 1K
R2 4K7
BC827 T1
R8 88R
J2
SPEAKER

NTE_68

commodore, bsw			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC PC EMULATOR		
APPROVED: H. ULLRICH			
USED ON: A2088	SIZE A3	380 756	REV A



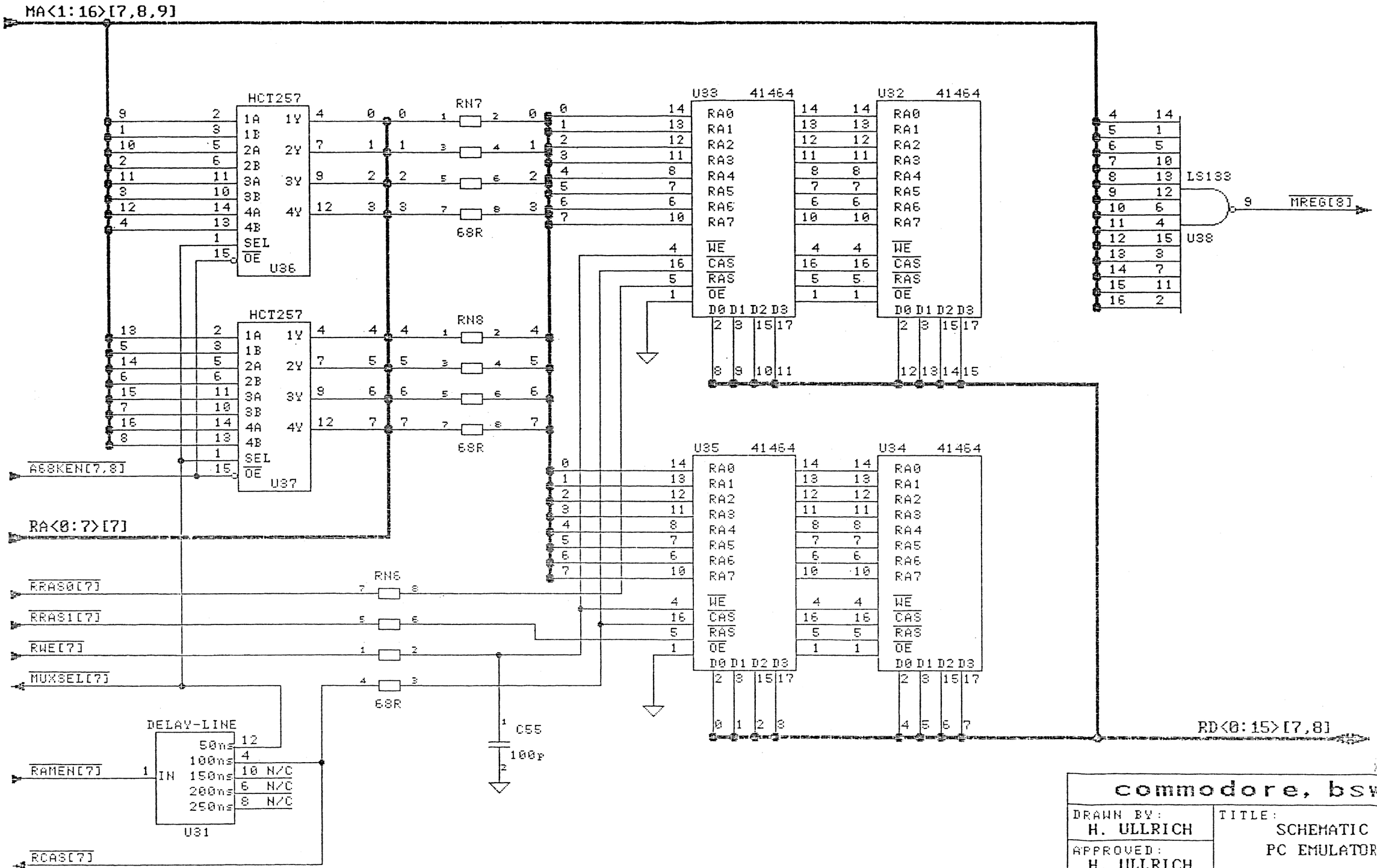
commodore, bsw			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC PC EMULATOR		
APPROVED: H. ULLRICH			
USED ON: A2000	SIZE A3	380 756	REV A



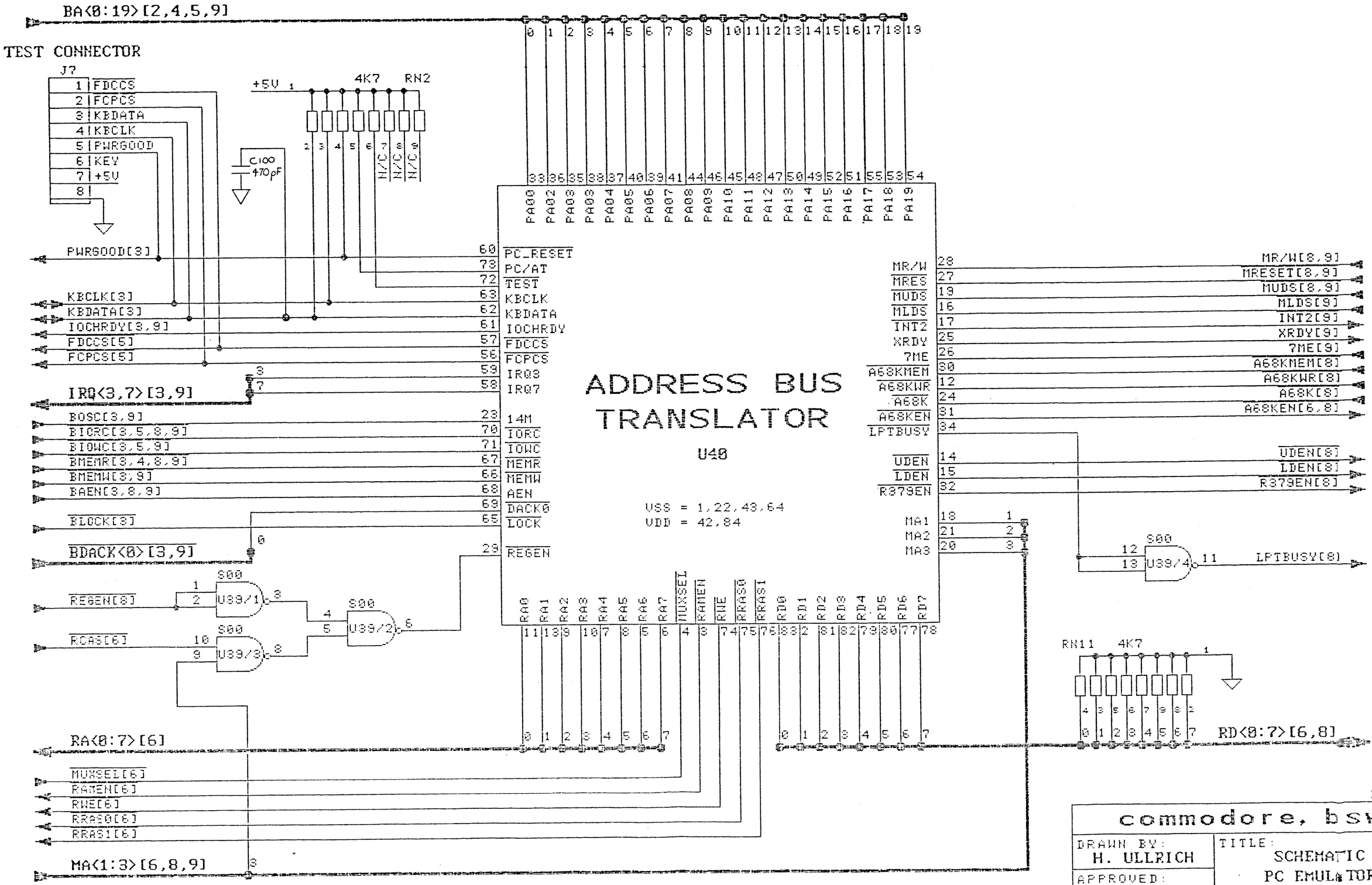
NOTES: JS1A-JS1F SELECT

XTE_65

commodore, bsw			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC PC EMULATOR		
APPROVED: H. ULLRICH			
USED ON: A 2000	SIZE A3	380 756	REV A

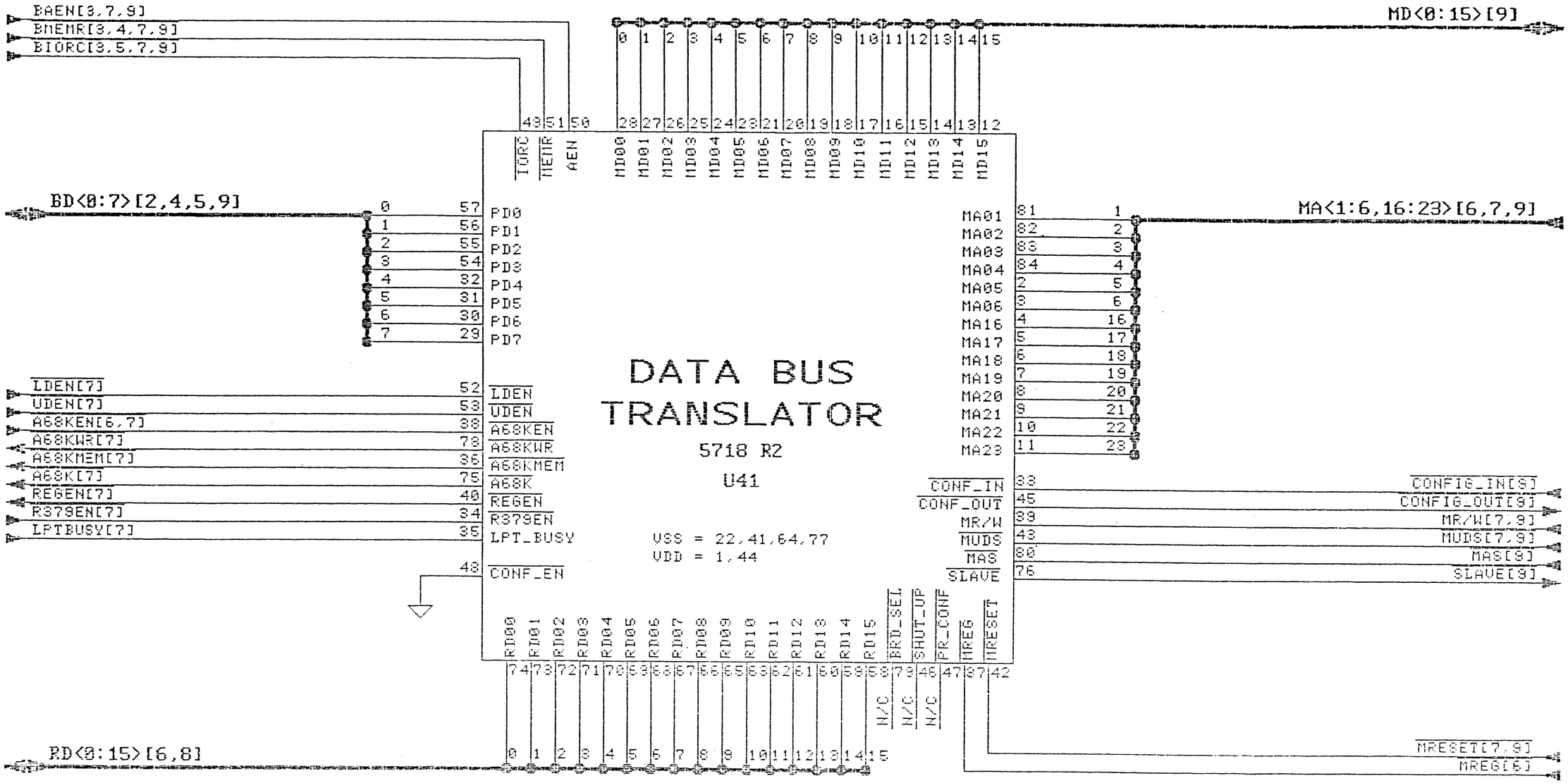


commodore, bsw			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC PC EMULATOR		
APPROVED: H. ULLRICH			
USED ON: A2000	SIZE A3	380 756	REV A



XTE_67

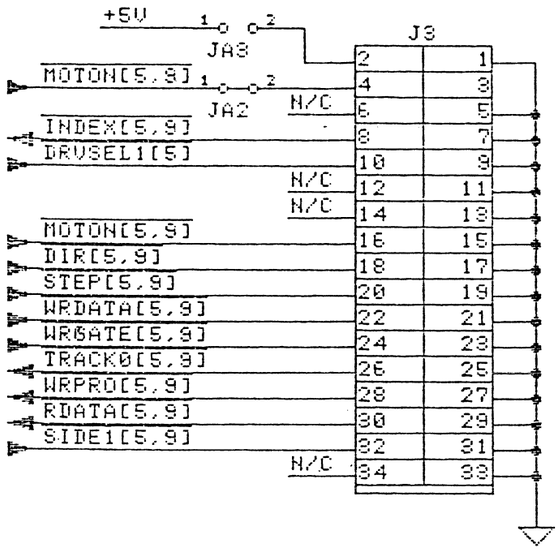
commodore, bsw			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC PC EMULATOR		
APPROVED: H. ULLRICH			
USED ON: A2088	SIZE A3	390756	REV A



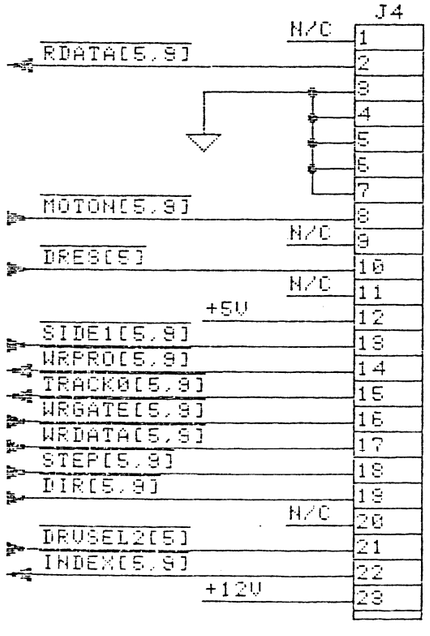
NTE_68

commodore, bsw			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC PC EMULATOR		
APPROVED: H. ULLRICH			
USED ON: A2088	SIZE A3	388 756	REV A

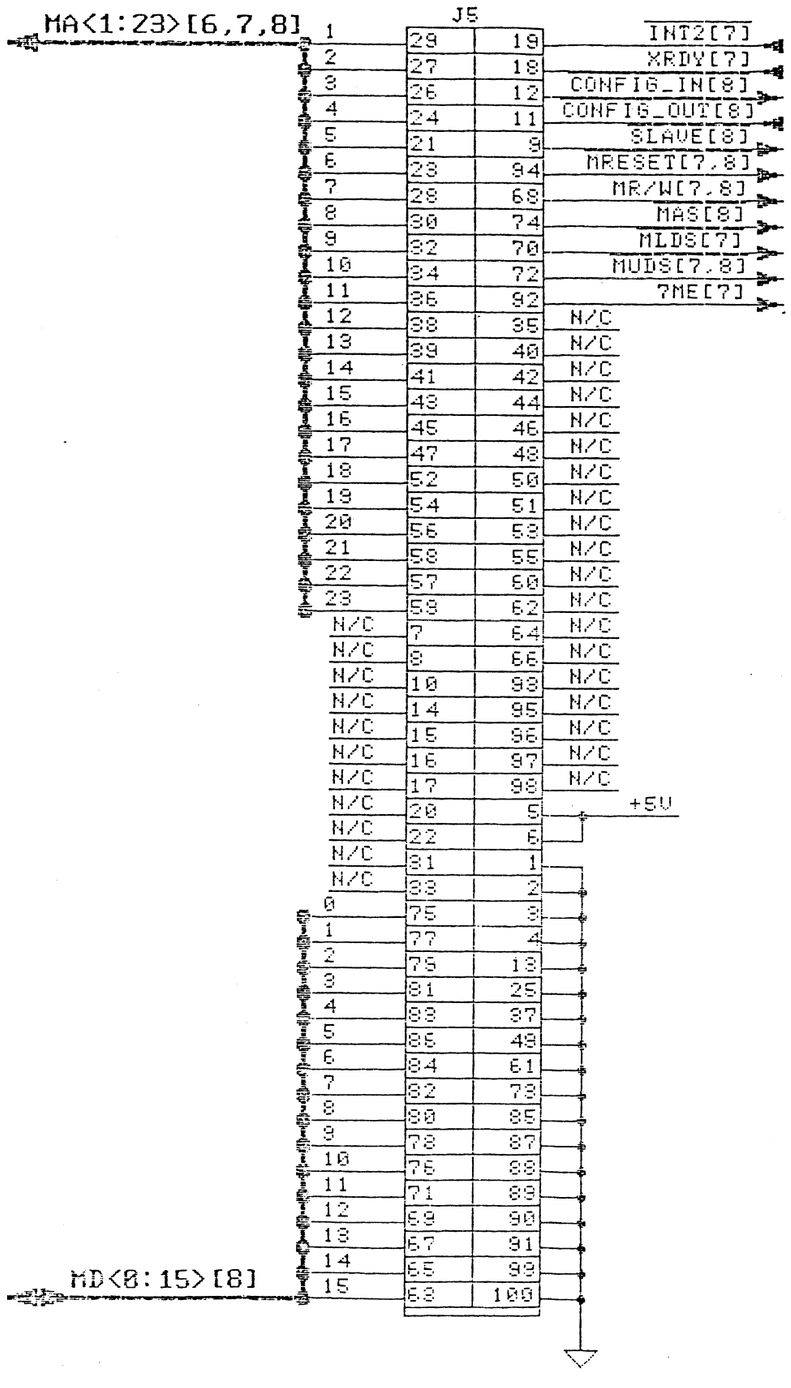
INTERNAL DRIVE (DRIVE A:)



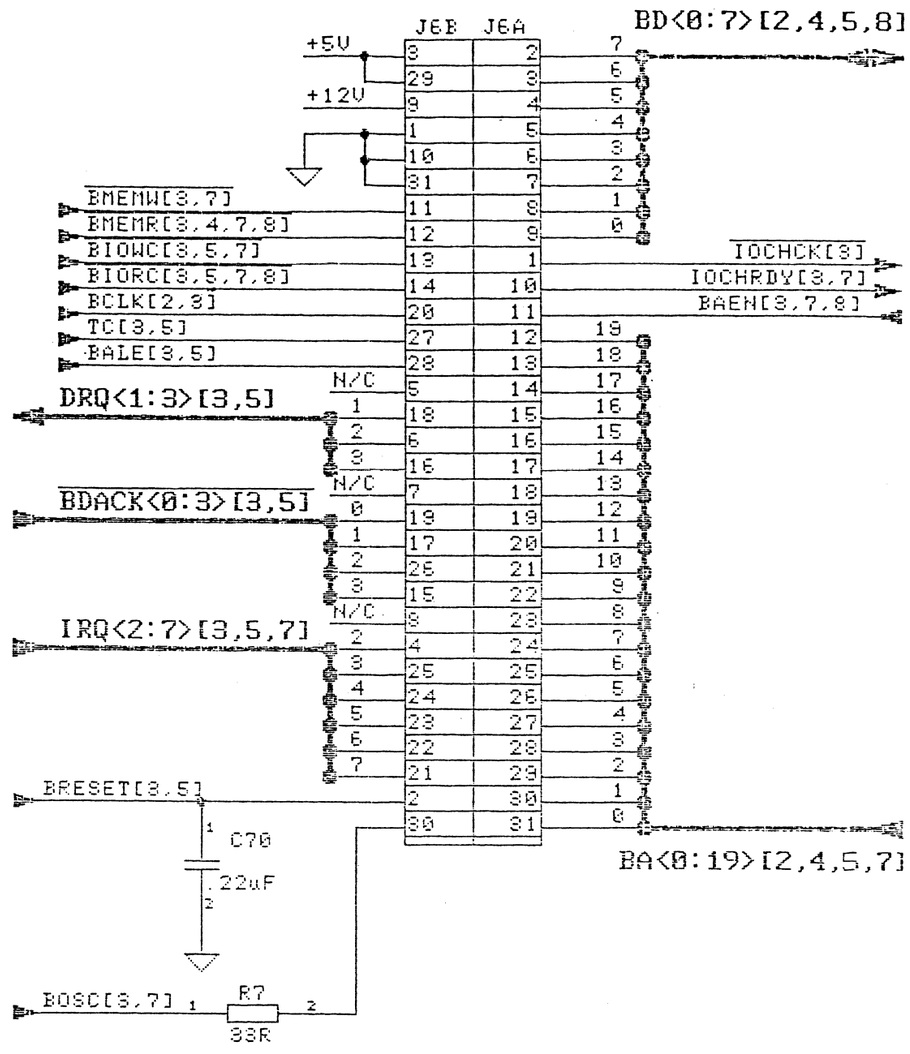
EXTERNAL DRIVE (DRIVE B:) 23 PIN SUBD CONN.



100 PIN A2000 BUS CARDEDGE CONN.



2x31 PIN PC BUS CARDEDGE CONN.

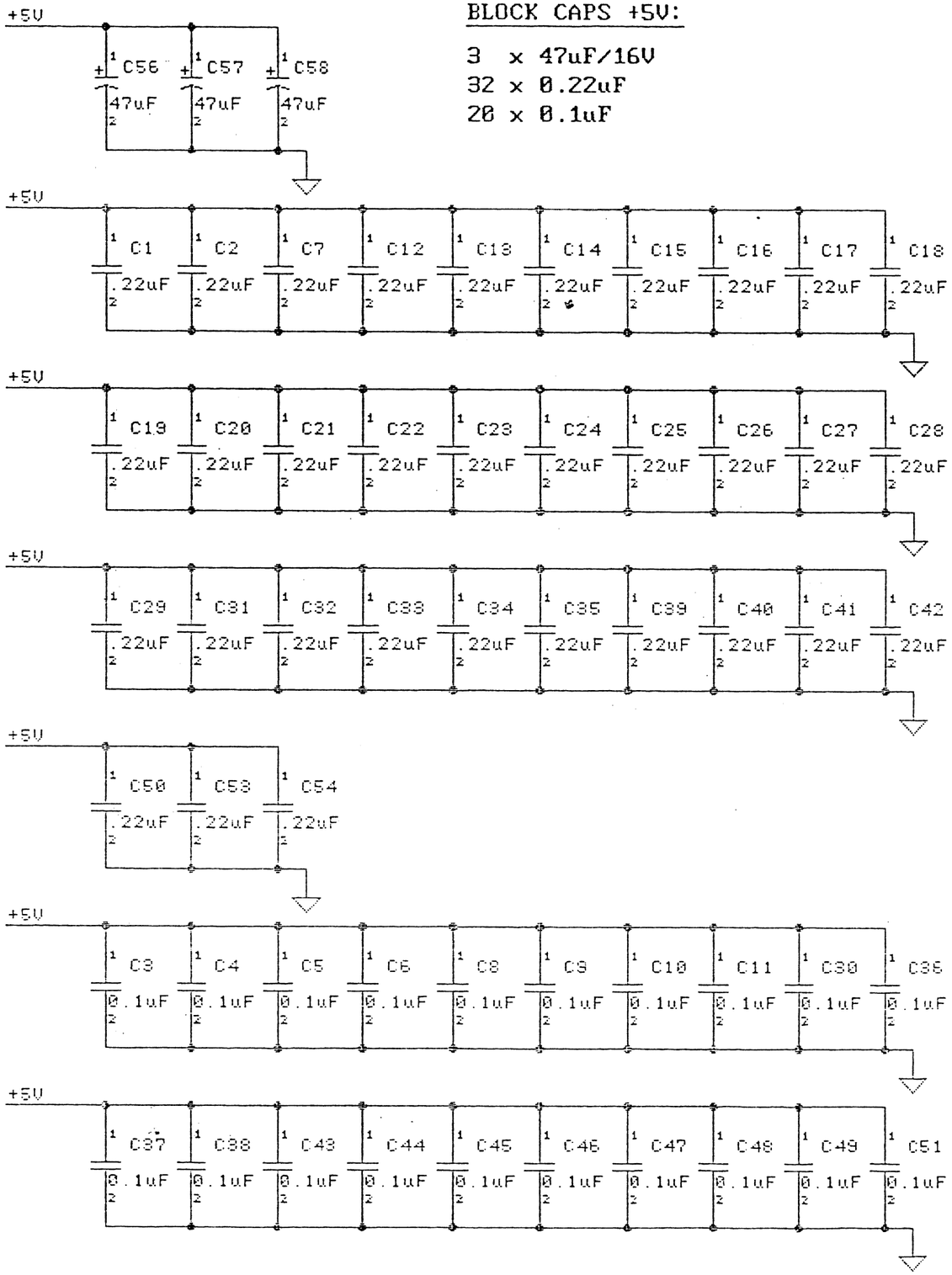


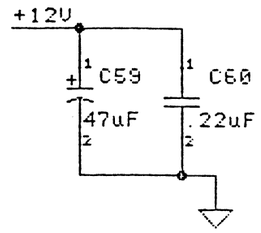
XTE_69

commodore, bsw	
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC PC EMULATOR
APPROVED: H. ULLRICH	
USED ON: A2000	SIZE A3 / 380 756 / REV A

BLOCK CAPS +5V:

3 x 47uF/16V
32 x 0.22uF
20 x 0.1uF

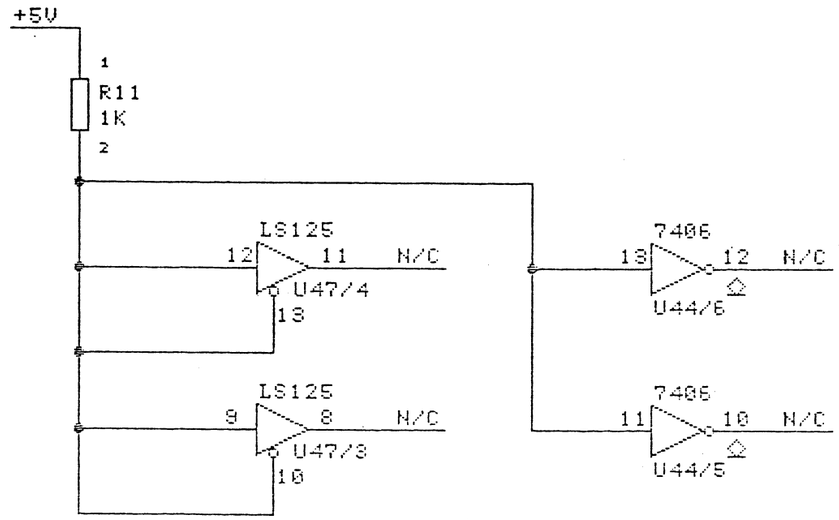




BLOCK CAPS +12V:

1 x 47uF/25V
1 x 0.22uF

SPARE GATES:



XIE_610

commodore, bsw			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC PC EMULATOR		
APPROVED: H. ULLRICH			
USED ON: A2000	SIZE A3	390 756	REV A

SCOPE

These Specifications apply to 5-1/4" double-sided 48-TPI minifloppy disk drive (hereafter abbreviated as FDD) CHINON F-502LII

FEATURES

The features of the F-502LII

(1) Pop-up Mechanism
With the newly employed pop-up mechanism, the disk can be loaded/unloaded with ease, preventing mischucking at disk insertion.

(2) Low Power Consumption
As a newly designed LSI (C-MOS chip) is employed in the read/write and control circuits, high performance and low power consumption are achieved. In stand-by mode, power consumption is only 1.86W, and in operation mode 4.42W, making system design easy.

(3) Built-in Disk-in-sensor
With the built-in disk-in-sensor, when no disk is loaded, the motor is stopped. This extends the motor service life and reduces power consumption. When chucking the disk, the DD motor is rotated temporarily to assure the centering of the disk.

(4) Automatic Power-down Control
If no rotation commands are sent to the step motor during a given period of time, the step motor will automatically go into a "power-save" mode.

(5) Direct Drive Brushless Spindle Motor
A slim, durable, direct drive spindle motor is used and even after continuous use, no maintenance or check procedures are required.

(6) Plug Compatibility
Recording format, data transfer rate and disk rotation speed are compatible with standard size 5-1/4" drives.

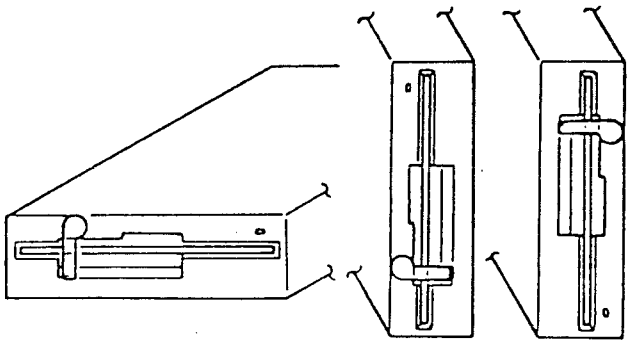
SPECIFICATIONS

Item			Specification	
			Double density	Single density
Storage capacity	Unformatted	Per disk	500 K bytes	250 K bytes
		Per track	6.25 K bytes	3.125 K bytes
	Formatted (16 sectors) (Equivalent to IBM format)	Per disk	327.68 K bytes	163.84 K bytes
		Per track	4096 bytes	2048 bytes
	Formatted (9 sectors) (Equivalent to IBM format)	Per disk	368.64 K bytes	184.32 K bytes
		Per track	4608 bytes	2304 bytes
Recording density			5876 BPI	2938 BPI
Rate of data transfer			250 K bits per second	125 K bits per second
Access time	Power-on to ready time		0.5 sec. or less	
	Single track seek time		5 ms per track	
	Average access time		86 ms	
	Settling time		20 ms	
	Average latency time		100 ms	
Rotation speed Long term speed variation Instantaneous speed variation			300 rpm Less than +1.5% Less than +1.5%	
Number of tracks			80	
Number of cylinders			40	
Number of heads			2	
Radius of track	Outer Inner		0 side: 57.151 mm 36.513 mm	1 side: 55.034 mm 34.396 mm
Number of indexes			1	
Recording mode			MFM	FM
Track density			48 TPI	

Specification

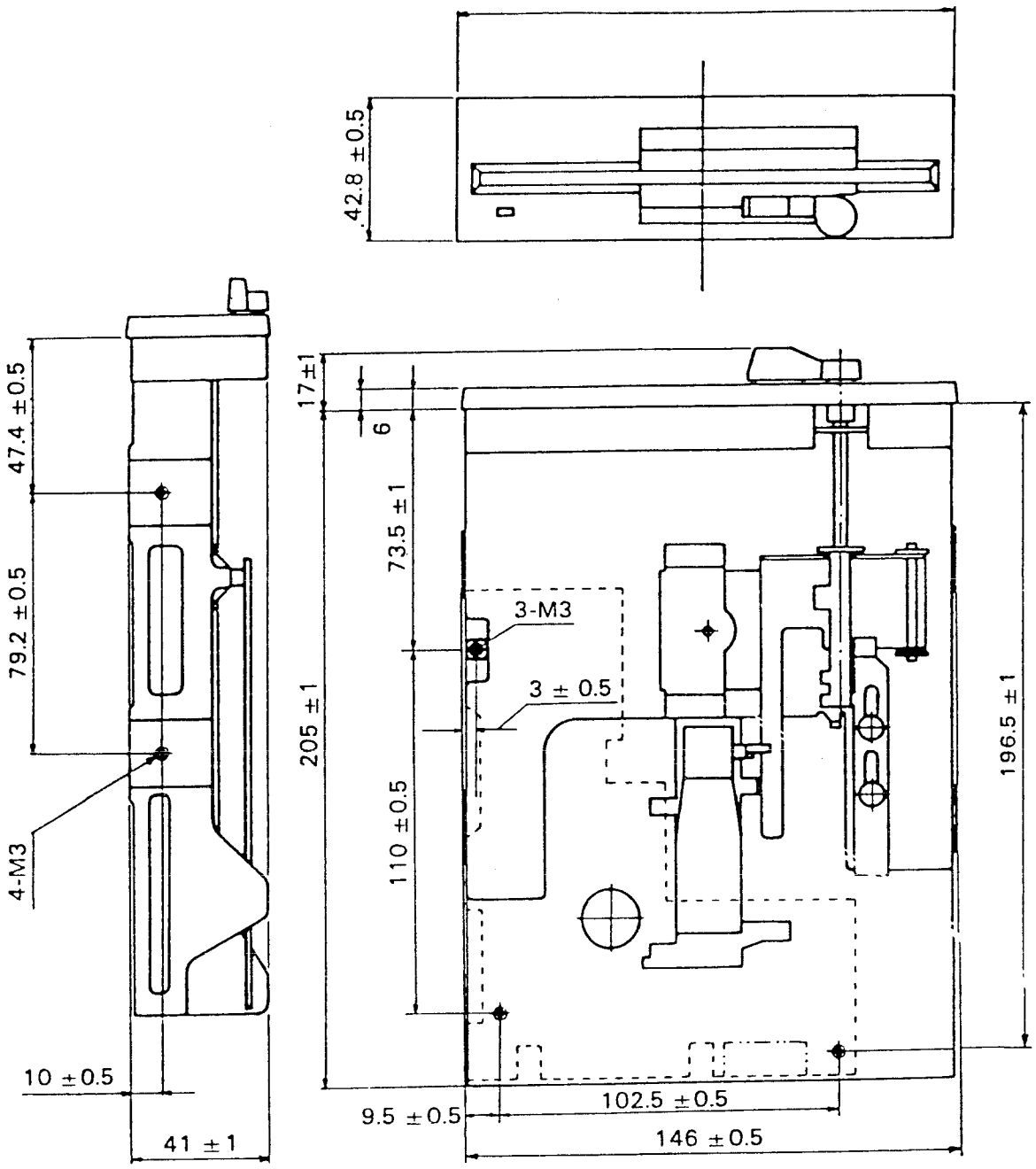
Item	Specification			
Physical dimensions	146 (W) x 41 (H) x 220 (D) mm			
Weight	Approx. 1.2 kg			
Power supply	DC +12 V ± 5%			
	DC +5 V ± 5%			
Power consumption		+5 V	+12 V	POWER
	Stand-by (DD motor off)	300 mA TYP.	30 mA TYP.	1.86 W TYP.
	Read operation	370 mA TYP.	160 mA TYP.	3.77 W TYP.
	Write operation	380 mA TYP.	210 mA TYP.	4.42 W TYP.
	Seek (continuance)	270 mA TYP.	500 mA TYP.	7.35 W TYP.
	Spindle Motor Starting current (0.5 sec. max.)		900 mA MAX.	
Ripple voltage allowance	DC +12 V	Less than 150 mVp-p (including spike noise)		
	DC +5 V	Less than 100 mVp-p (including spike noise)		
Noise	Less than 55 phons (class A) (separated from the drive by 1 m)			
Cabinet specifications	Front panel	Material: ABS Color: Light Grey(See below)		
	Front lever	Material: ABS Color: Light Grey(See Below)		
		Maker : Shin-Nittetsu Chemical Industries. P/N : BK-8052KW-5		

Installation Conditions

<table>
<tr><th>Item</th><th colspan="4">Specification</th></tr>
<tr><td>Mounting position</td><td colspan="4"> 
Horizontal Vertical
Keep the horizontal level to within 15 degrees with front panel raised.</td></tr>
<tr><td rowspan="6">Environment conditions</td><td rowspan="3">Temperature</td><td>During operation</td><td colspan="2">5 ~ 45°C</td></tr>
<tr><td>During non-operation</td><td colspan="2">0 ~ 50°C</td></tr>
<tr><td>During storage</td><td colspan="2">-20 ~ 60°C</td></tr>
<tr><td rowspan="3">Humidity</td><td>During operation</td><td colspan="2">20 ~ 80% RH Maximum wet bulb temperature 29°C</td></tr>
<tr><td>During non-operation</td><td colspan="2">5 ~ 90% RH No dew condensation</td></tr>
<tr><td>During storage</td><td colspan="2">8 ~ 90% RH No dew condensation</td></tr>
<tr><td colspan="2">Temperature change</td><td colspan="2">15°C/H</td></tr>
<tr><td rowspan="4">Vibration</td><td rowspan="2">During operation</td><td>Continuous vibration</td><td>Amplitude Less than 0.5 mm 5 ~ 25 Hz
0.25G 25 ~ 100 Hz</td></tr>
<tr><td>Single vibration</td><td>Less than 10G (10 ms)</td></tr>
<tr><td rowspan="2">During non-operation and storage (W/Protect sheet)</td><td>Continuous vibration</td><td>Amplitude Less than 7 mm 5 ~ 9 Hz
0.5G 9 ~ 100 Hz</td></tr>
<tr><td>Single vibration</td><td>Less than 30G (10 ms)</td></tr>
<tr><td>Drop shock</td><td colspan="4">Fall height in packing State: 70 cm
(corner: one time, sides: three times, flat surfaces: six times)</td></tr>
</table>

DIMENSIONS

Dimension for F-502LII



INTERFACE SIGNALS

The interface signal has 11 input signal lines and 5 output signal lines. See Fig. 5-1.

Signal Voltage Levels

The interface signal interfaces with the controller at the TTL level. For all signals, low is true. The I/O signal level into the drives have the following specifications.

(1) Input signal
- Low level 0V to +0.40V
- High level +2.40V to +5.25V
- Input impedance 150Ω

(2) Output signal
- Low level 0V to +0.40V
- High level +5.25V max. (by receiving the end terminator)
- Output current (for low level) 48 mA (max.)
- Output current (for high level) 250 μA (max.)

Input Signals

(1) DRIVE SELECT 0 to 3 signal lines

When one of these signal lines goes into low level, the drive corresponding to the signal line is selected and the I/O gate is opened. Up to four drives can be controlled using these four signal lines. The drive corresponding to one of the DRIVE SELECT 0 to 3 signal lines is determined by the position of the short plug in the drive.

This line also controls the ON/OFF of the spindle motor. When one of the DRIVE SELECT 0 to 3 goes into low level, the spindle motor revolves. When it is set to high level, it stops.

(2) DIRECTION SELECT signal line

This signal determines the direction of movement of the head when a pulse is sent via the STEP signal line. When this signal line is set to low level and the STEP signal pulse is sent, the head moves toward the center of the disk. When it is set to high level and the STEP signal pulse is sent, the head moves away from the center.

The logic level of this signal should be held for at least 1 microsecond after the trailing edge of the STEP pulse.

(3) STEP signal line

This signal line moves the head. With the rise of a single low level pulse, this signal line changes from LOW level to HIGH level and the head moves one track in the direction determined by the DIRECTION SELECT signal.

However, this signal is not accepted when the FDD is in WRITE mode. The head is stabilized 20 ms after the trailing edge of the last STEP pulse, and the FDD is ready for data read/write operation.

(4) WRITE GATE signal line

This signal line specifies drive write and read status. When this signal line is set to low level, write enable status occurs and the data is stored on the disk surface by the WRITE DATA signal. When this signal line is set to high level, read status occurs.

After the writing operation, a period of 1.2 ms is necessary before a valid READ DATA signal appears on the interface.

(5) WRITE DATE signal line

Data written on the disk surface is transferred on this signal line. With the decline of the pulse sent to this signal line (when the signal line changes from the high level to the low level), data is written on the disk surface.

(6) SIDE SELECT signal line

This signal line selects the head.

When this signal line is set to high level, the side 0 head is selected; when it is set to low level, the side 1 head is selected. Side 0 stands for the one-sided medium recording surface.

The selection is completed 100 microseconds after the change of the SIDE SELECT signal line, and read/write becomes possible.

Output Signals

(1) INDEX signal line

Whenever the disk rotates once, this signal line outputs a low level pulse indicating the start of the track. A decline of the pulse signal (when this signal line changes from high level to low level) indicates the start of the track. However, the pulse is only output when the disk is inserted.

(2) TRACK 00 signal line

When this signal line is set to low level, the head is located at the track 00 position and the specific phase of the stepping motor is excited.

(3) WRITE PROTECT signal line

When this signal line is set to low level, the inserted disk cannot be written on. This signal line may also be set to low level even when no disk is inserted in the drive. The write function of the drive becomes inoperative when write-inhibited disk is inserted.

(4) READ DATA signal line

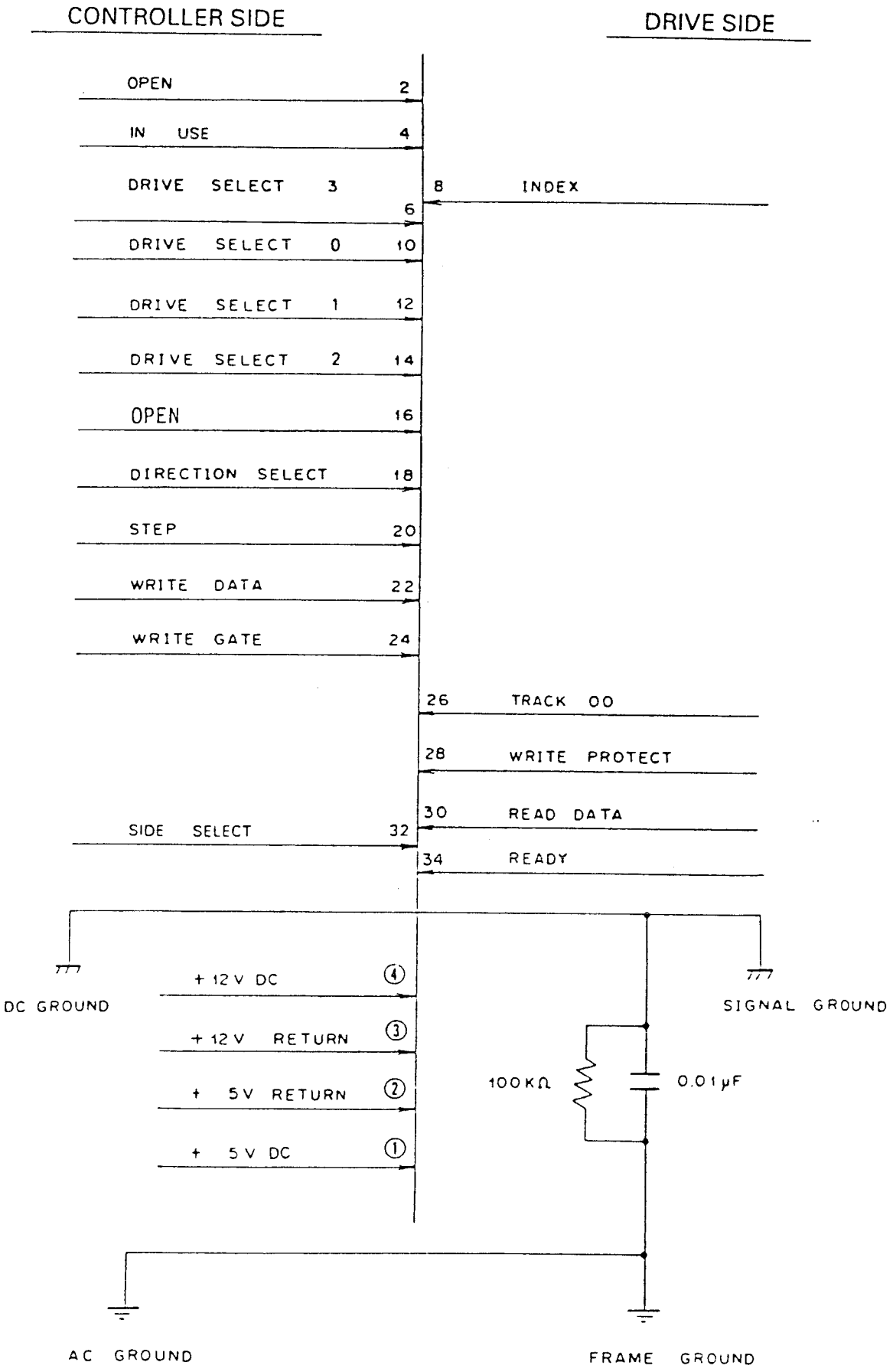
This signal line is used for the transfer of the pulse series read from the disk, in which clock pulses and data pulses are mixed. The negative-going edge (the moment of change from high level to low level) of the pulse output at this signal line indicates the readout data (clock and data pulses). (See Page 14.)

(5) READY signal line

When this output signal line is set to low level, the disk is inserted and the number of disk rotations is fixed.

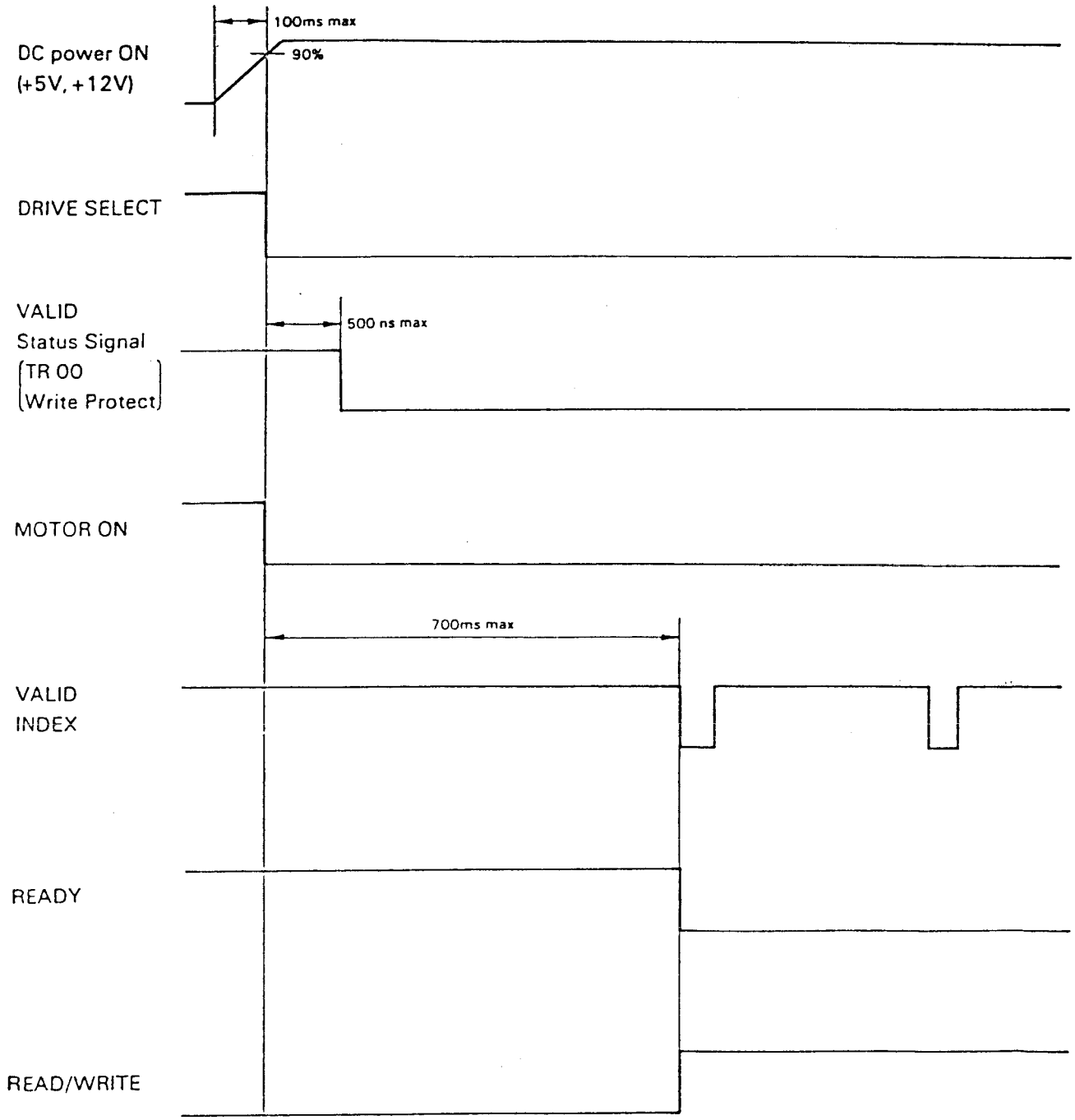
When the READY signal is ON, read and write operations can be performed on the disk. Immediately after the MOTOR ON signal is turned ON, power is supplied. After the disk is inserted, check that the READY signal is ON before performing write and read operations.

Fig. 5-1 Interface with the controller and host system

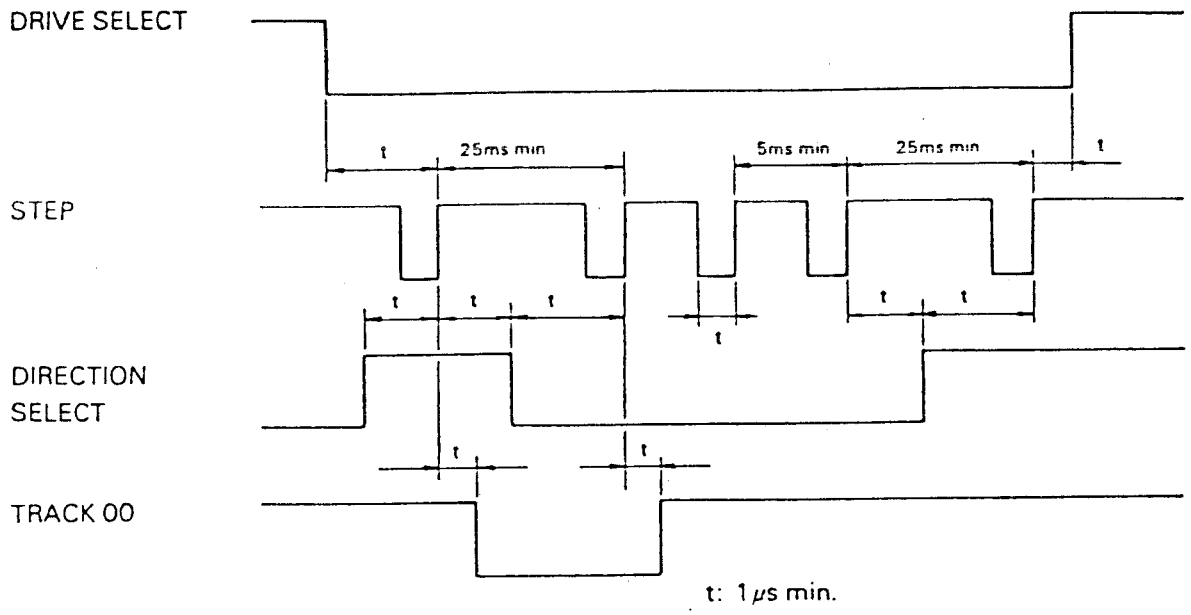


Signal Timing

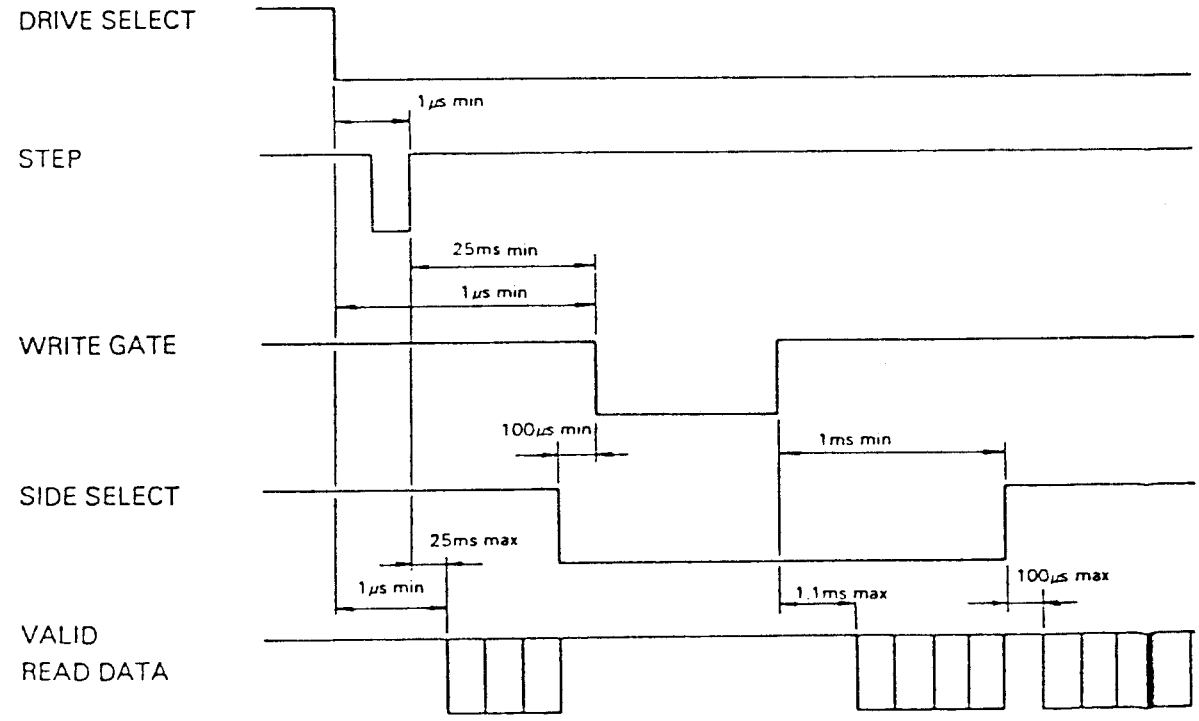
(1) Initialize sequence



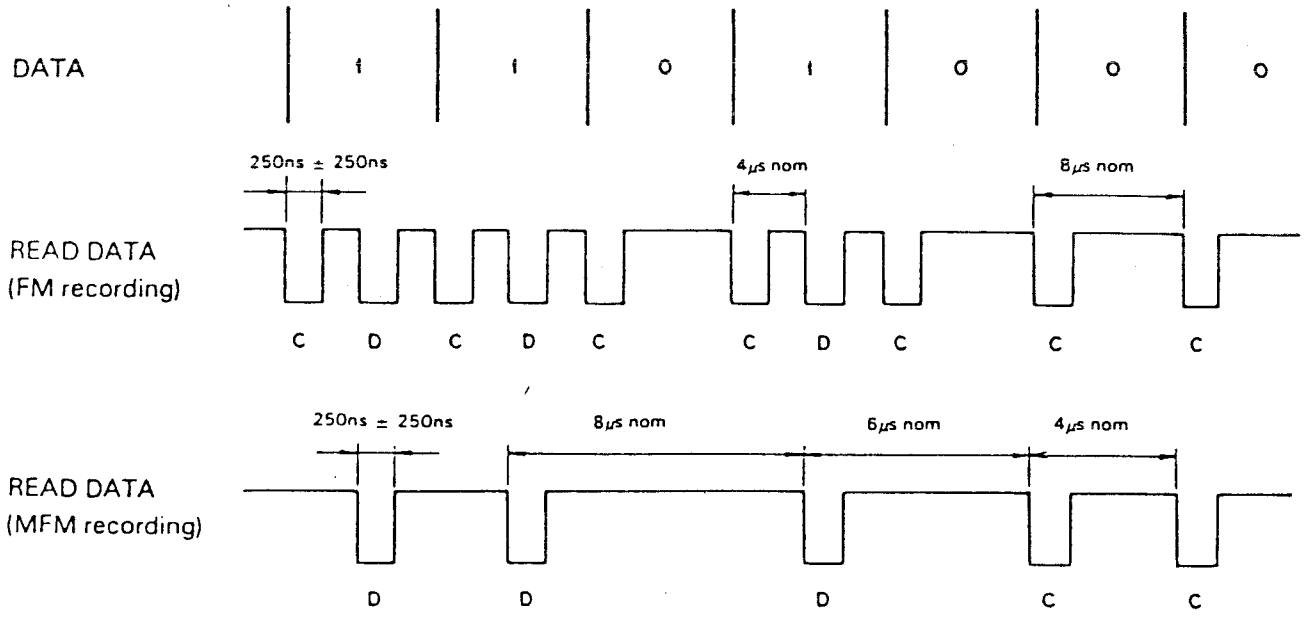
(2) Access timing



(3) Read timing

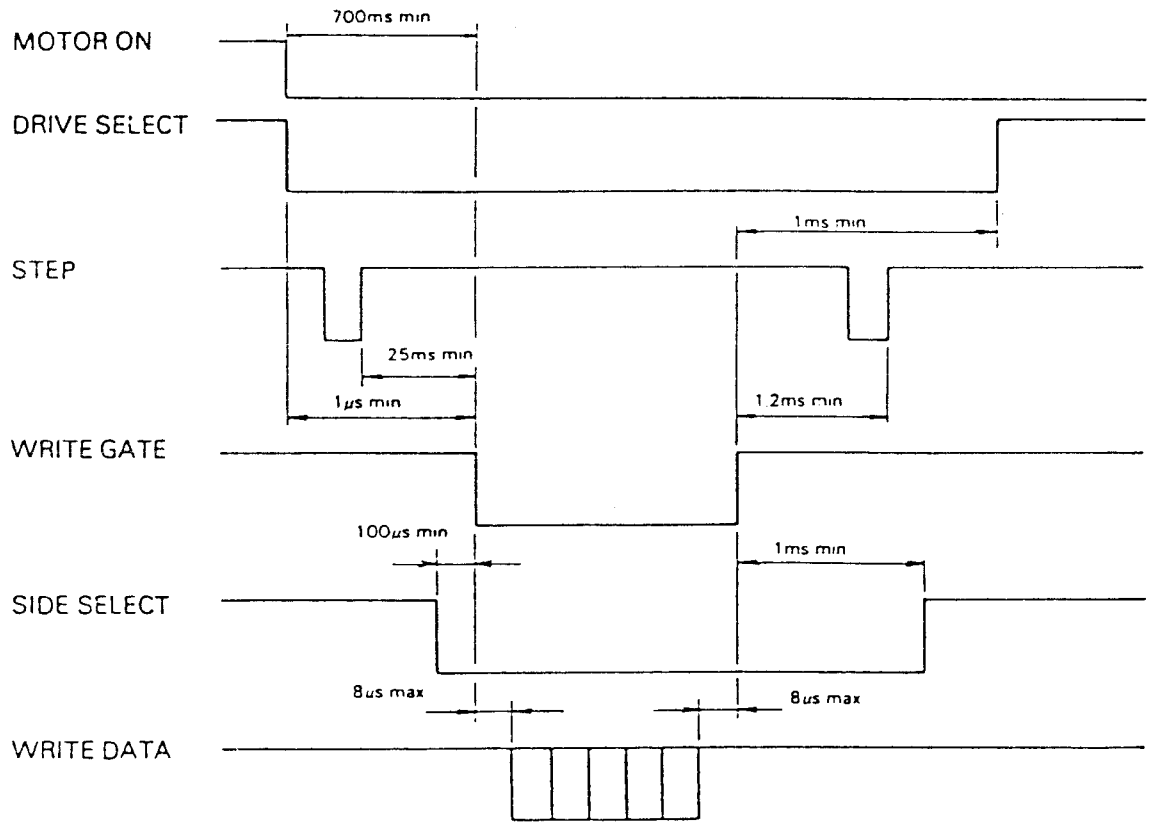


(4) READ DATA timing

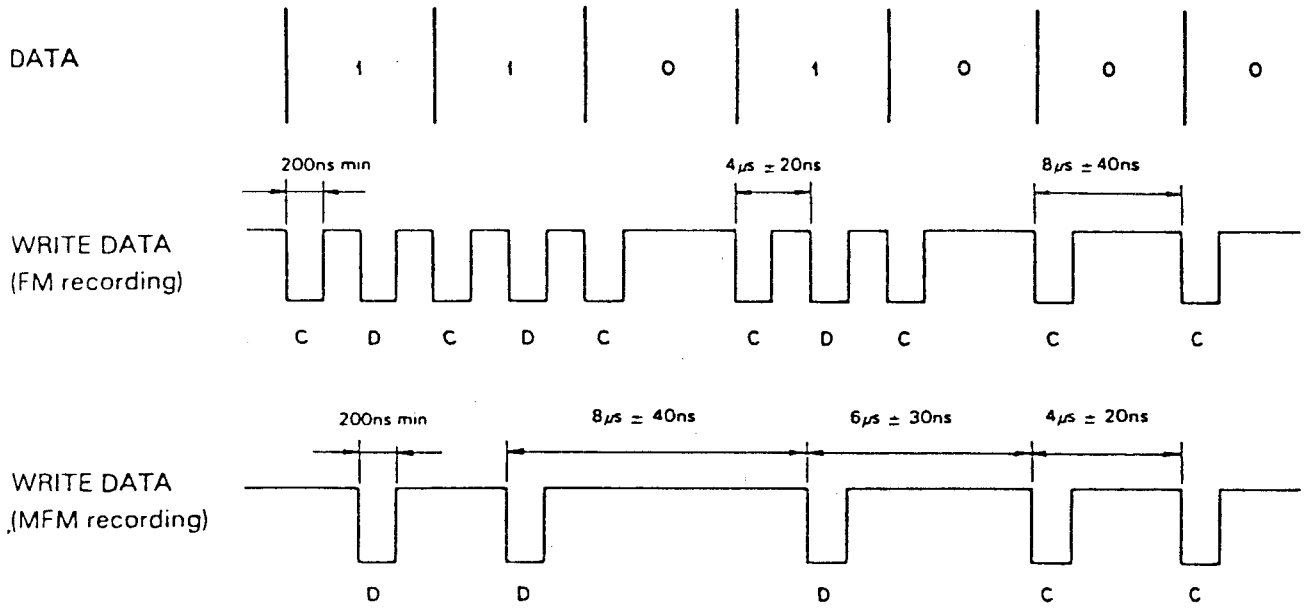


C; Clock D; Data

(5) Write timing

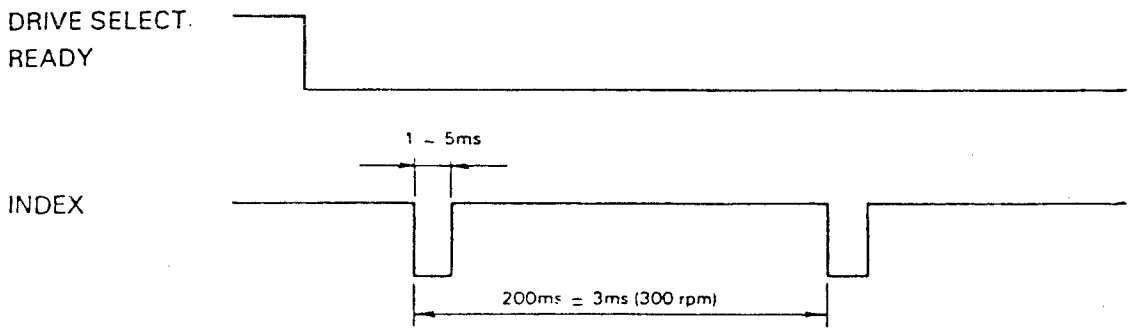


(6) WRITE DATA timing



C: Clock D: Data

(7) INDEX timing



POWER SUPPLY INTERFACE

Power Supply Specifications

The DC power (+12V, +5V) shown in Specification (2) of Section 3-2 is required by the power supply. There are four power lines (+12V, +5V, and the two return lines).

Frame Ground

The frame ground and signal ground are connected through a capacitor and a resistor. The values are as follows:

$R = 100\ k\Omega$ $C = 0.01\ \mu F$

Connect the frame ground where the AC ground and DC ground are one point connected in the host system.

Power Supply Sequence

(1) The power ON sequence is not specified. However, the time in which the supplied power voltage rises up to 90% of the specified value, should be set to 100 ms or less.

(2) If the drive is in a status other than write operation, and the DC power is disconnected, the disk and the data stored on the disk are not destroyed. However, its contents will be destroyed if the WRITE GATE is not set to high level.

INTERFACE CONNECTOR AND PIN ARRANGEMENT

Interface Connector

(1) DC power connector

	Drive side	Host side
Connector/housing	AMP 172349-1 or equivalent	AMP 1-480424-0 or equivalent
Pin	———	AMP 60619-1 or equivalent

(2) Interface signal connector

	Drive side
Connector	Card Edge Connector (Fig. 8-2)

Pin Arrangement

The arrangement of each pin is shown Fig. 7-1. This diagram shows the back of the drive.

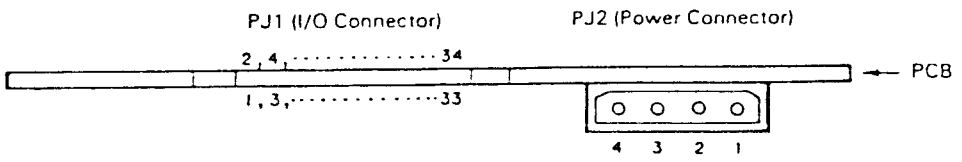


Fig. 7-1 Pin Arrangement

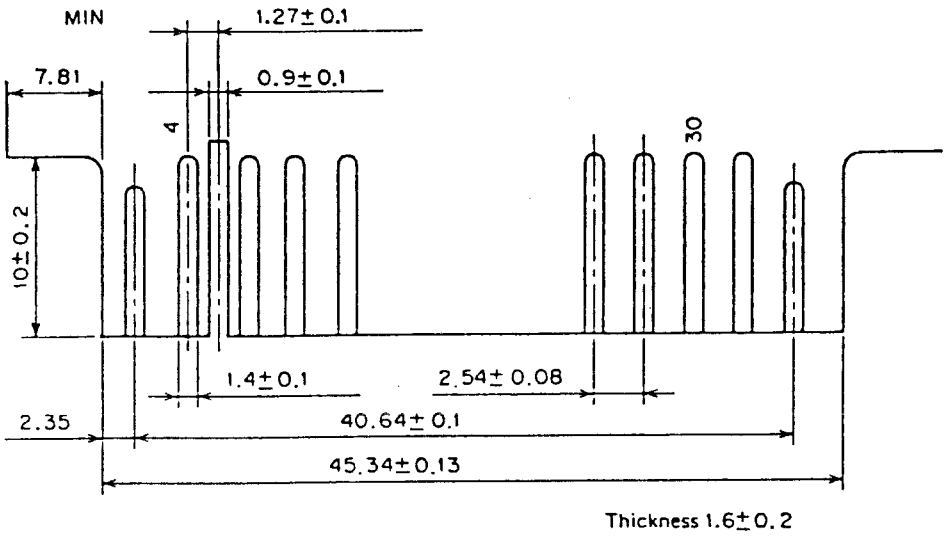


Fig. 7-2 Card Edge Connector

(1) DC Power connector

Pin number	Signal
1	+12V DC
2	+12V RETURN
3	+5V RETURN
4	+5V DC

(2) Interface signal connector

Pin number	Signal	Pin number	Signal
2	OPEN	1	GND
4	IN USE	3	GND
6	DRIVE SELECT 3	5	GND
8	INDEX	7	GND
10	DRIVE SELECT 0	9	GND
12	DRIVE SELECT 1	11	GND
14	DRIVE SELECT 2	13	GND
16	OPEN	15	GND
18	DIRECTION SELECT	17	GND
20	STEP	19	GND
22	WRITE DATA	21	GND
24	WRITE GATE	23	GND
26	TRACK 00	25	GND
28	WRITE PROTECT	27	GND
30	READ DATA	29	GND
32	SIDE SELECT	31	GND
34	READY	33	GND

GND: SIGNAL GROUND

SHORT PLUG AND FRONT LED

Short Plug

The arrangement of each pin is shown Fig.

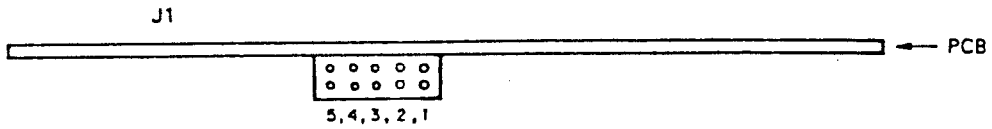


Fig. 8-1 Short Plug

This diagram shows the side of the drive.

Note: Position 1 through 5 of the "J1" are designated as follows.

POS. 1: Connect the termination resistors when closed
POS. 2: Configure the drive as "DRIVE 0" when closed
POS. 3: Configure the drive as "DRIVE 1" when closed
POS. 4: Configure the drive as "DRIVE 2" when closed
POS. 5: Configure the drive as "DRIVE 3" when closed

Front LED

The front LED lights when the DRIVE SELECT signal selected by the short plug is set to low level.

Functions of Test Points

The following ten test points (with two GND) are provided on the control board, each of which is used in observing the waveform for FDD adjustment or check.

(1) TP1, TP2 (pre-amp output) and TP3 (analog GND)

These are the test points of the read amp output.

The signal from the head, after being amplified in level about 200 times by the pre-amp, and then filtered out by an LPF, after which it can be observed at test points TP1 and TP2. TP1 and TP2 are in 180° anti-phase to each other.

For accurate waveform observation, it is necessary to add the signals of both channels together (the signal of the one channel is inverted in phase) to observe these signals as one waveform using an oscilloscope with two channels. TP3 is used in grounding the oscilloscope.

TP1 and TP2 are used in checking the read/write head for its different characteristics or in checking and adjusting the tracking alignment, the index burst timing.

(2) TP4 (read data signal)

This is the test point of the read data pulse. The inverted READ DATA signal appears here.

In FM mode, a data signal with 2F or 1F period is observed, while in MFM mode, a data signal with 2F, 1.5F or 1F period is observed. (See Table 106.)

This test point is used in check and adjustment of asymmetry.

(3) TP5 (Digital GND)

(4) TP6 (index sensor)

This is the test point of the index sensor photo-transistor output after it passes through the Schmitt inverter. Thus the inverted output signal appears at this test point.

TP6 is used in the following checks and adjustments.

1. Check and adjust disk rotating speed
2. Check and adjust index burst timing
3. For external trigger check and adjust tracking alignment

(5) TP7 (index sensor)

This is the test point of the index sensor photo-transistor output. A waveform with soft leading and trailing edges appears here, since the sensor output signal is taken out before flowing across the Schmitt inverter. Here it is necessary to check that the output voltage of the index sensor is normal (with no waveform split).

Note: Use TP6 in check and adjustment of index burst timing since the index burst timing may deviate according to its relevant manner of triggering.

(6) TP8 (write protect sensor)

This is the test point of the write protect sensor photo-transistor output. The inverted WRITE PROTECT output signal appears here. With a disk in which a measure for write protection is taken (its notches are masked), it becomes high level.

The voltage at this test point should be more than 3 V in the write protect state and less than 0.5 V in the write enable state (the notches are open).

This test point is used in check and adjustment of the write protect sensor.

(7) TP9 (Disk-in sensor)

This is the test point of the disk-in sensor photo-transistor output.

This signal becomes high level when a disk is inserted into the FDD

(8) TP10 (track 00 sensor)
This is the test point of the track 00 sensor photo-transistor output. The voltage at this test point should be within the range shown in Fig. 107.

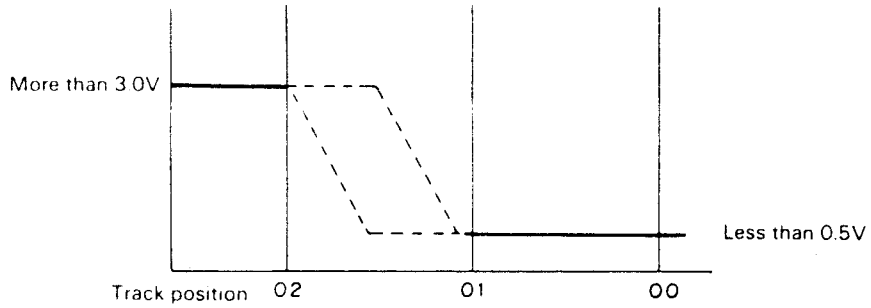


Fig. 107

Adjust so that the level of the sensor output changes between track 01 (Low level) and track 02 (High level).

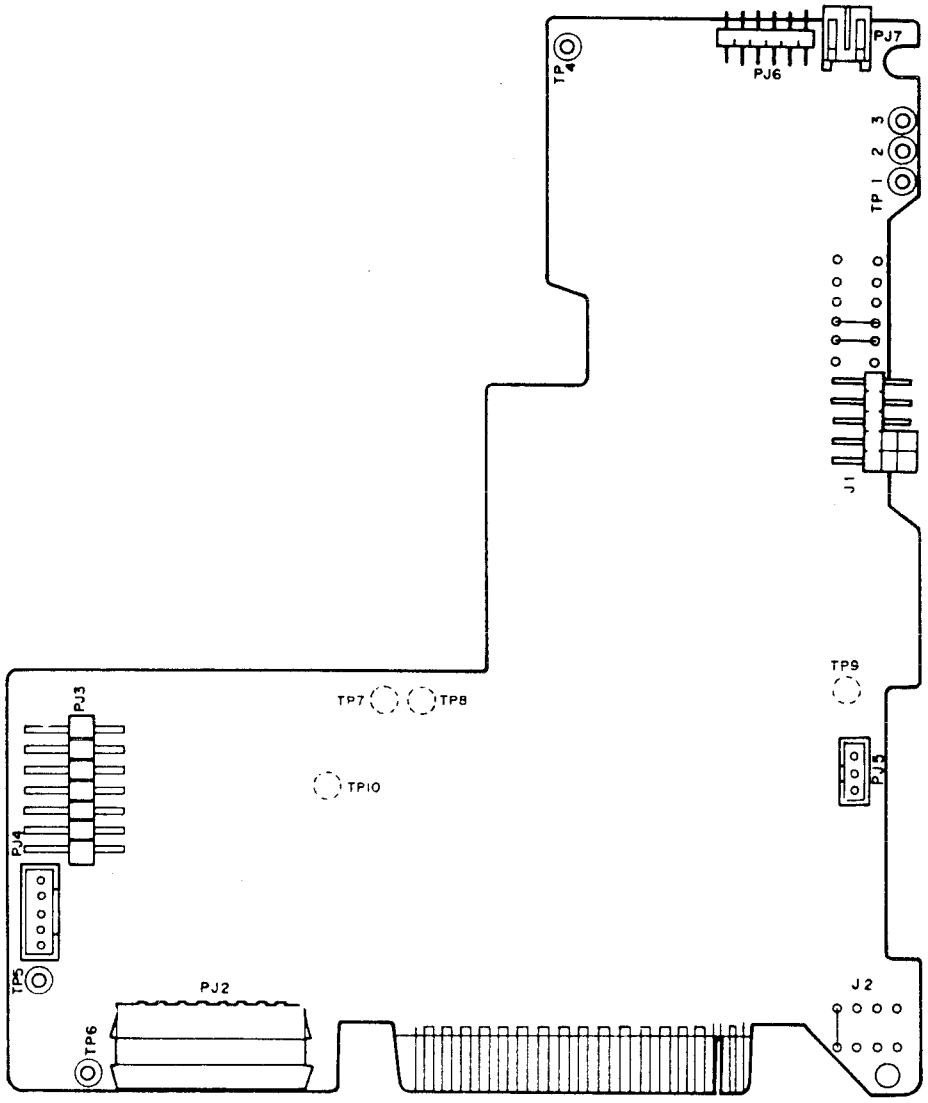


Fig. 108 Test points and connectors on the control PC board ass'y

Check and Adjustment

Adjustment of Veil Position (For F-502II)

When the clamp base plate ass'y is replaced or when the machine is repaired, adjust the position of the veil as follows:

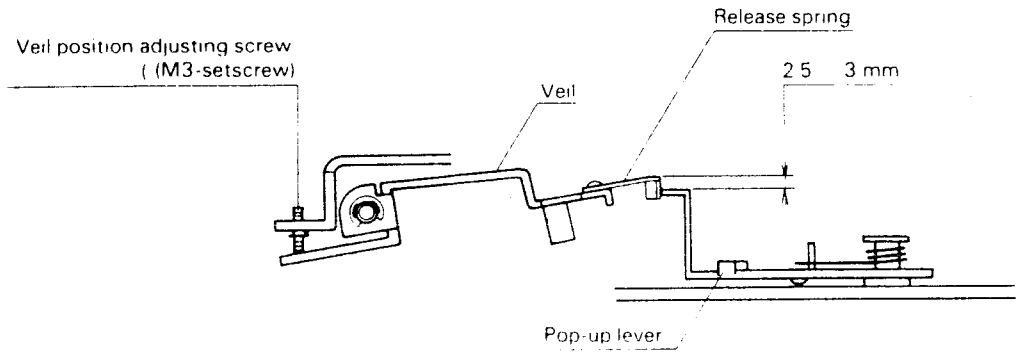
(1) Tools

① Hex. wrench for M1.5

① Screw lock adhesive

(2) Check and adjustment procedure

1. Lift the door lever (Fig. 408) to release the lock.
   (The door lever should be kept opened.)
2. Load the work disk (do not close the door lever).
3. Turn the veil adjusting screw so that the distance between the release spring and pop up lever when they start moving is 2.5 ~ 3 mm (Fig. 301).
4. If the value specified in item 3 cannot be obtained, adjust the veil adjusting screw.
5. Apply screw lock to the veil adjusting screw.
6. For setscrew mounting, refer to item 1-2-1.



Adjustment of Clamp Support Plate Position

When the following parts are replaced or when the machine is serviced, adjust the position of the clamp support as follows:

- ○ Clamp base plate ass'y
- ○ Clamper ass'y
- ○ DD motor ass'y

(1) Tools

① Phillips screwdriver for M2.5

② Screw lock adhesive

(2) Adjustment (This adjustment is not needed on F-502LII Rev.B.)

1. Push down the door lever (Fig. 408) to lock. In case of F-502LII, set the pop-up lever to the disk insertion position (Fig. 409) and set the front lever as shown in the right figure to lock.
2. Loosen two clamp support mounting screws.
3. Adjust the position of the clamp support and align the holes in the clamper guide and clamper shaft.
4. Tighten the screws to the specified torque and apply a small amount of screw lock adhesive. See Fig. 302.

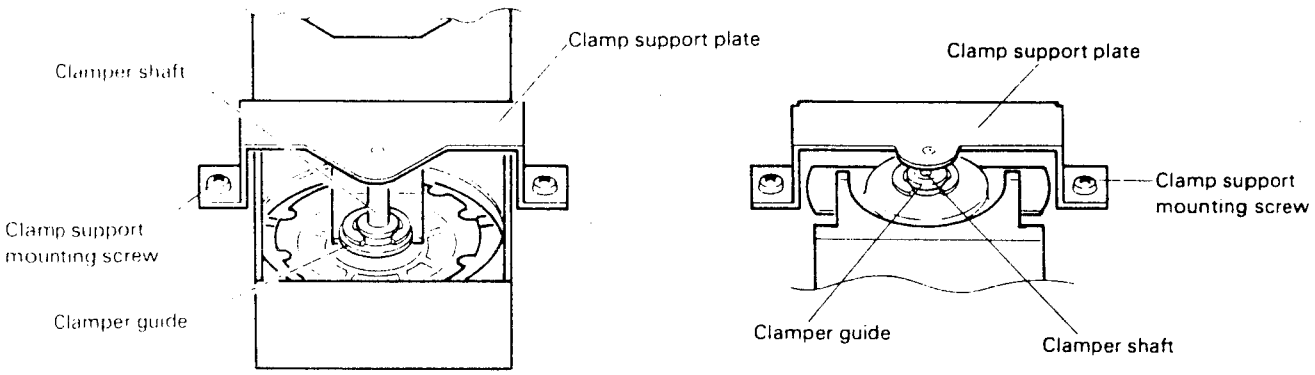


Fig. 302

Check of Write Protect Sensor

When replacing the following assemblies, be sure to check the write protect sensor.

- ○ DD motor ass'y
- ○ Write protect sensor ass'y

(1) Measuring instruments and jigs

① Max. media jig

② Digital voltmeter or oscilloscope

③ FDD tester

(2) Check procedure

1. Connect the digital voltmeter or oscilloscope to test point TP8 on the control PC board.
   Setting of oscilloscope: DC 1 V/div.
2. Insert the max. media jig at the position where notch A is on the path of the light from the write protect sensor.

3. Supply power to the FDD, then check that the voltage at TP8 is within the following range:
   Voltage at TP8 when notch A is on the light path: Less than 0.5V
4. Shift the max. media jig to the position where notch B is on the path of the light.
5. Supply power to the FDD, then check that the voltage at TP8 is within the following range:
   Voltage at TP8 when notch B is on the light path: More than 3.0V
6. When it is not within the specified range, check whether or not there is foreign matter on the light path. If so, remove it. If not, replace the write protect sensor ass'y in accordance with item 4-11.

Check of Disk-in Sensor

When replacing the disk-in sensor ass'y, be sure to check the disk-in sensor.

(1) Measuring instruments
   ① Work disk
   ② Digital voltmeter or oscilloscope
   ③ FDD tester

(2) Check procedure
1. Connect the digital voltmeter or oscilloscope to test point TP9 on the control PC board ass'y.
   Setting of oscilloscope: DC 1V/div.
2. Supply power to FDD, then check that the voltage at TP9 is within the following range:
   Voltage at TP9: Less than 0.5V
3. Insert the work disk and supply power to FDD, then check that the voltage at TP9 is within the following range:
   Voltage at TP9 when inserted work disk: More than 3V
4. When it is not within the specified range, check whether or not there is foreign matter on the light path. If so, remove it. If not, replace the disk-in sensor ass'y in accordance with item 4-14.

Check and Adjustment of Disk Rotating Speed

The rotating speed of the DD motor has been adjusted berore the DD motor ass'y is built in. When replacing or repairing this ass'y check and adjust the disk rotating speed according to the following procedure:

(1) Measuring instruments, and tools
   ① Small screwdriver
   ② Frequency counter
   ③ Work disk
   ④ FDD tester

(2) Check and adjustment procedure
1. Connect the frequency counter to TP6 and TP5.
2. Load the work disk and rotate the DD motor.
3. Set the head to track 00.
4. Check that separation between pulses at TP6 is within the following range:
   Pulse separation at TP6: 200 ± 3 ms
5. When the pulse separation is not within the specified range, adjust the variable resistor (see Fig. 412) on the servo PC board of the DD motor ass'y so that it is set to around the center value of the specified range.

Check and Adjustment of Head for Touching with Disk

When replacing or repairing the following parts or assemblies, check and adjust the head for touching with the disk according to the following procedure:

○ Head carriage ass'y

(1) Measuring instruments and tools

①Oscilloscope
②FDD tester
③Work disk

(2) Check and adjustment procedure

1. Connect the oscilloscope to TP1 or TP2 (pre-amp output).
   Setting of oscilloscope: AC 0. 2 V/div., 20 msec/div.
2. Load the work disk and rotate the DD motor.
3. Move the head to track 39.
4. Select the side 0.
5. Write one cycle of a 2F signal, then set the FDD in reproduction mode.
6. Measure the average read level for the above one cycle.
7. Pressing the upper section of the head arm very lightly (10 ~ 20 gram), execute step 5 and measure the read level as in step 6.
8. Check that the average read level at step 6 is more than 80% of the read level at step 7.
9. Select the side 1 and repeat items 5 ~ 8.
10. Move the head to track 00, then execute steps 4 ~ 9.
11. If the value specified in item 6 cannot be obtained, loosen the veil adjusting screw (Fig. 408) (by about 90°) and check again. After re-adjustment, be sure to check and adjust the veil position referring to item 3-1. (For F-502II)
12. When the requirement in step 6 is not met even by executing step 11, the following causes can be assumed.
    a. Disk defective:
       When the disk or jacket is deformed or damaged, replace the work disk.
    b. Head carriage ass'y defective:
       Replace it in accordance with item 4-9.

Note: When pressing the head arm, be careful not to lower the rotating speed of the DD motor by pressing it with excessive force.

Check and Adjustment of Asymmetry

When replacing the following assemblies, check and adjust the asymmetry according to the following procedure:

○ Head carriage ass'y
○ Control PC board ass'y

(1) Measuring instruments and tools

①Oscilloscope
②Alignment disk
③FDD tester
④Small screwdriver
⑤Work disk

(2) Check and adjustment procedure

1. Connect the oscilloscope to TP4 on the control PC board.
   Setting of oscilloscope: DC 1 V/div.
2. Load the alignment disk and rotate the DD motor.

3. Move the head to track 39.
4. Select the side 0.
5. Check that the asymmetry meets the following value:
   Asymmetry (with alignment disk): Less than 0.6 μsec.
   Arrange so that three read data pulses can be observed on the oscilloscope screen. Then, check so that the split (asymmetry) width of the second read data pulse waveform from the trigger pulse.
6. Remove the alignment disk and load the work disk.
7. Write a 1F signal on track 39 and measure the split (asymmetry) width of the waveform as shown in Fig. 303.
8. Check that the asymmetry meets the following value:
   Asymmetry of 1F signal on track 39: Less than 0. 6 μsec
9. Select the side 1 and repeat items 5 ~ 8.
10. When the asymmetry does not meet the specified value, the following causes can be assumed.
    a. Disk defective:
       Replace the work disk.
    b. With high density of leak magnetic flux around FDD:
       When magnetic flux sources such as magnet, transformer, CRT, magnetizied iron, etc. are near the FDD, place them far away, then carry out the asymmetry check and adjustment once again
    c. Head defective:
       Replace the head carriage ass'y in accordance with item 4-9.
    d. Read amp defective:
       Replace the control PC board ass'y in accordance with item 4-3.

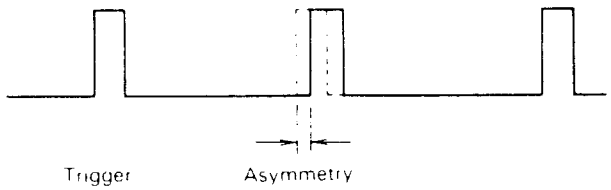


Fig. 303

Check of Read Level and Resolution

When replacing the following assemblies, check the read level and resolution.

○ Head carriage ass'y
○ Control PC board ass'y

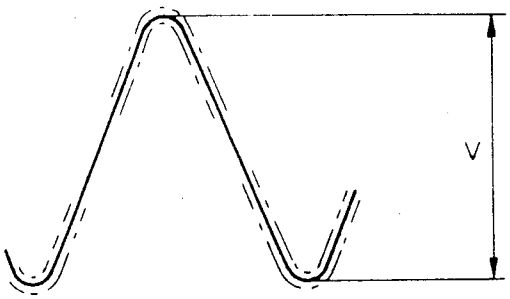
(1) Measuring instruments
   ① Oscilloscope
   ② FDD tester
   ③ Reference disk

(2) Check procedure

1. Connect the two channel oscilloscope to TP1 and TP2 (each for pre-amp output) on the control PC board.

   Setting of oscilloscope: AC 0.1 V/div, 2 ∿ 5 μs/div.

   Set channels CH1 and CH2 both to the above range, invert the signal of either channel and add the signal of both channels together.
2. Load the reference disk and rotate the DD motor.
3. Move the head to track 39.
4. Select the side 0.
5. Write one cycle of a 2F signal and measure the average read level. (See Fig. 304)



V: Average read level

Fig. 304

6. Put the read level in step 5 and the calibration value of the reference disk in the following equation, then calculate the true value of the read level.

   (True value of read level = average read level + calibration value)
7. Check that the true value of the read level meets the following value:

   Read level of 2F signal on track 39: More than 400 mVp-p
8. Write one cycle of a 1F signal with the above condition maintained, measure the average read level and find the true value of the read level in accordance with step 6.
9. Put the read levels of 1F and 2F signals in the following equation, and resolve.

$$\text{Resolution (true value)} = \frac{\text{read level of 2F signal (true value)}}{\text{read level of 1F signal (true value)}} \times 100\%$$

10. Check that the resolution meets the following value:

    Resolution on track 39: More than 60%
11. Select the side 1 and repeat items 5 ~ 10.
12. When the true value of the read level in step 7 and/or the result in step 10 does not meet the specified values, the following causes can be assumed.

    a. Reference disk defective:

       When the disk or the jacket is deformed or damaged, replace the reference disk.

    b. Improper rotation of disk:

       Check and adjust the rotating speed of the disk in accordance with item 3-5.

    c. Improper touching of head with disk:

       Check and adjust the head for touching with the disk in accordance with item 3-6.

    d. Head defective:

       Replace the head carriage ass'y in accordance with item 4-9.

    e. Control PC board read/write amp defective:

       Replace the control PC board in accordance with item 4-3.
13. Remove the reference disk.

Check and Adjustment of Tracking Alignment

When replacing the following assemblies or part, be sure to check and adjust the tracking alignment.

- ○ Head carriage ass'y
- ○ Stepping motor ass'y
- ○ Steel belt
- ○ DD motor ass'y
- ○ Clamper ass'y

(1) Measuring instruments and tools

- ① Two channel oscilloscope
- ② Alignment disk
- ③ FDD tester
- ④ Phillips screwdriver for M3
- ⑤ Screw lock adhesive
- ⑥ Thermometer and hygrometer

(2) Check procedure

Check and adjust the tracking alignment at normal room temperature (about 23°C) and humidity (about 50%). Avoid check and adjustment under extreme environmental condition even when temperature and humidity are within the permissible ranges specified for the FDD and disk, because tracking adjustment may not be done exactly under such conditions. In addition, when the FDD and the alignment disk (CE disk) are left for more than two hours, until their temperatures are balanced with the normal environmental temperature, higher accuracy can be obtained. It is recommended that adjustment be made with the FDD in the same position as when housed in the system.

Similarly, it is advisable to use an alignment disk which has been checked for calibration (provided with correction data) with the standard drive. In addition, note that use of an alignment disk which has exceeded its life may cause inaccurate adjustment.

1. Connect the two channel oscilloscope to TP1 and TP2. Connect the external trigger input to TP6 (index sensor output).

   Setting of oscilloscope:
   CHI: AC 0.5 V/div., 20 msec/div.
   CH2: AC 0.5 V/div., 20 msec/div., inverted
   Others: Both outputs added together and external trigger used on the (+) trigger setting.

2. Rotate the DD motor and load the alignment disk.
3. Select the side 0
4. Move the head to alignment check track 16.
5. Check that the burst signal wave form in Fig. 305 is observed. If the burst signal wave form is not observed,the tracking is out of alignment.
   Adjust the tracking alignment.

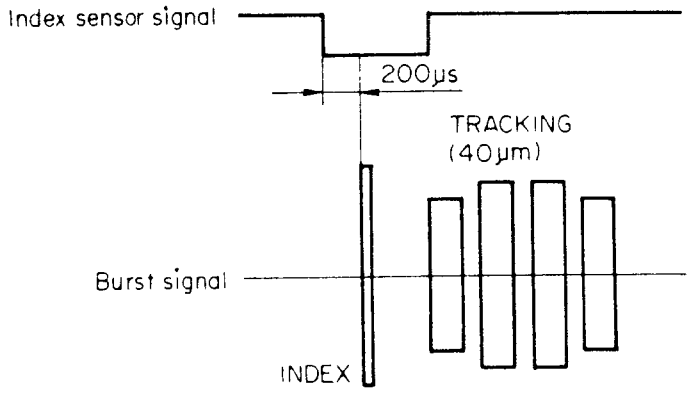


Fig. 305

6. After stepping in the head by one or several tracks from the original track position, step it out by the same number of steps to return it to the set track position, then measure values B1 to B4. Calculate the off-track amount as follows. (See Fig. 306)

   Off-track amount (μm) = 2K.(B2−B3)/(B2+B3−B1−B4)

   K = 40 μm

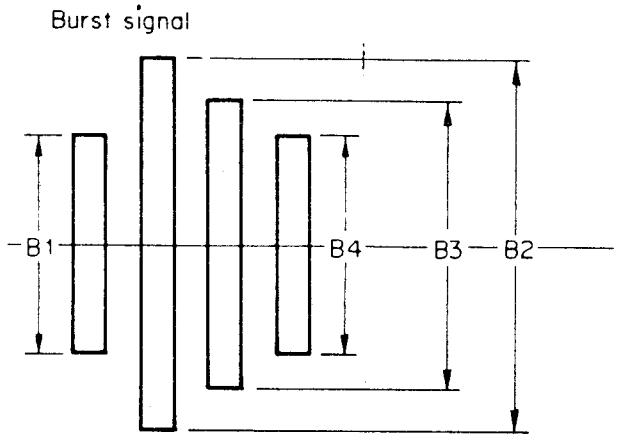


Fig. 306

7. After stepping out the head by one or several tracks from the original track position, step it in by the same number of steps to return it to the set track position, then measure values B1 to B4. Calculate the off-track amount in the same manner as item 6.
8. Select the side 1 and repeat items 4 ~ 7.
9. Check that the respective off-track amounts in items 6 and 7 are within the following range. when they are not within the specified range, adjust the tracking according to the adjustment procedure.

   Off-track amount (um) = ± 40μm

(3) Adjustment procedure

1. Loosen the stepping motor setscrews A and B. (Fig. 412)
2. Move the head to track 16.
3. Manually rotate the stepping motor body and monitor the burst signal waveform. (Fig. 305) When the burst signal waveform cannot be received, check with track 14 or 18.

   Note: To align with the excited phase of the stepping motor, be sure to move the head to an odd number track.
4. When the burst signal waveform is located, rotate the stepping motor body so that the right and left peak points of B2 and B3 become the same as the calibrated value. Then, secure the motor.
5. Step the head in and out repeatedly, and fine adjust the installation of the stepping motor so that the alignment error (difference between B2 and B3) of the burst signal waveform is minimized when the head is returned to the alignment check track inward and outward. When hystereses occur in inwards and outwards trackings, adjust so that both hystereses are equal.
6. Perform the same procedures on sides 0 and 1 so that the alignment error of the sides 0 and 1 becomes minimum.
7. Tighten the stepping motor retaining screws A and B in this order to a specified torque and repeat adjustment so that the alignment error is within ± 40 μm.
8. Apply screw lock to the stepping motor retaining screws.
9. Remove the alignment disk.
10. Adjust the track 00 sensor, referring to item 3-10.
11. Adjust the track 00 stopper, referring to item 3-11.

Check and Adjustment of Track 00 Sensor

When adjusting or replacing the following assemblies or part, check and adjust the track 00 sensor.

- ○ Head carriage ass'y
- ○ Stepping motor ass'y
- ○ Steel belt
- ○ Track 00 sensor ass'y

(1) Measuring instruments and tools

- ① Oscilloscope
- ② Digital voltmeter
- ③ Alignment disk
- ④ FDD tester
- ⑤ Phillips screwdriver for M3
- ⑥ Screw lock adhesive

(2) Check procedure

1. Set up the oscilloscope referring to the steps in 3-9 "Check of tracking alignment", step 1.
2. Move the head to alignment check track 16 and check that a burst signal is received as shown in Fig. 305.
3. If the correct burst signal cannot be received, adjust as shown in "Adjustment".
4. Remove the alignment disk.
5. Connect the digital voltmeter or oscilloscope to TP10.
   Setting of oscilloscope: DC 1 V/div.
6. Start the DD motor and load the work media.
7. Check that the voltage at TP10 is as shown in the table when the head is moved to the specified position.

Track 00 ~ 01	Less than 0.5 V
Track 02 or subsequent tracks	More than 3.0 V

Table 307

   If the voltage at TP10 is not as specified in Table 307, adjust referring to "Adjustment".
8. Check that the voltage waveform at TP10 is not very much disturbed at HIGH-LOW switching when the head is repeatedly moved between tracks 00 and 04.

(3) Adjustment procedure

1. Connect the FDD tester with the tester connected, turn its power off once.
2. Connect the oscilloscope, referring to 3-9 "Check of tracking alignment", step 1.
3. Loosen the track 00 sensor mounting screw (Fig. 412) and fully move the track 00 sensor to the DD motor side.
4. Turn the FDD tester on, start the DD motor and load the alignment disk.
5. Repeat step in operation until burst signal waveform is observed (Fig. 305).
6. Fully move the track 00 sensor outward.
7. Step the head out by 15 tracks outward (track 01 position).
8. Measure the voltage at TP10 with digital voltmeter or oscilloscope.
9. Position the track 00 sensor so that the voltage at TP10 is "Low" level (less than 0.5 V).
10. Step the head in by 1 track (track 02 position).
11. Check that the voltage at TP10 is "High" level (more than 3 V).
12. If the correct voltage cannot be obtained, fine adjust the position of the track 00 sensor so that the voltage indicated in step 9 and 11 is obtained.
13. Tighten the mounting screw to the specified torque.

Check and Adjustment of Track 00 Stopper

When adjusting the tracking alignment or the track 00 sensor, be sure to check and adjust the track 00 stopper according to the following procedure:

(1) Measuring instruments and tools
   ① Pencil light (or flash light)
   ② FDD tester
   ③ Phillips screwdriver

(2) Check procedure
   1. Remove the three mounting screws and the one collar of the control PC board ass'y.
   2. Disconnect the two head connectors (PJ6), the front LED connector (PJ7) and the disk-in sensor connector (PJ5) from the control PC board ass'y and reverse the control PC board ass'y around 14-pin connector (PJ3). (See Fig.108)
   3. Move the head to track 00. In this condition, check that there is a very small clearance between the stepping motor pulley pin and the track 00 stopper (for F-502II/F-502LII Rev.A) or between the carriage ass'y and the track 00 stopper screw (for F-502LII Rev.B). (See Figs. 408 ~ 410)
   4. While directing the light of the pencil light (or flash light) onto the light receiver section (lower side) of the track 00 sensor, move the head outwards by one step (to track -01).
   5. Check that the stepping motor pulley pin or the head carriage (F-502LII Rev.B) touches the track 00 stopper with a sound after which it remains in contact with the stopper.
   6. As instructed in step 4, further more the head outwards by one steps (to track -02). At this time, check that the head carriage returns to its original position of track 00 with a very small clearance between the stepping motor pulley pin or the head carriage (for F-502LII Rev.B) and the track 00 stopper.
   7. Move the head inwards and outwards repeatedly between track 00 and the track located several tracks inside. At this time, check that no striking sound occurs between the stepping motor pulley pin or the head carriage (for F-502LII Rev.B) and track 00 stopper.
   8. Check by seeking track 39 that the pulley pin does not hit the track 00 stopper. (only F-502II/F-502LII Rev.A)
   9. When the requirements in step 3 ~ 8 are not met, adjust the track 00 stopper position according to the procedure in "Adjustment".

(3) Adjustment procedure
   1. Set the head to track 00.
   2. Loosen the mounting screw of the track 00 stopper. (only F-502II/F-502LII Rev.A)
   3. Adjust the stopper or stopper screw (F-502LII Rev.B) to the position at which there is a very small clearance between the pulley pin or the head carriage and stopper. Then, tighten the mounting screw of the stopper to the specified torque.
   4. Execute steps 3 ~ 8 in "Check".
   5. Attach the control PC board in the reverse procedure to that when detached.

Check and Adjustment of Index Burst Timing

When adjusting or replacing the following assemblies, be sure to check and adjust the index burst timing.

- Head carriage ass'y
- DD motor ass'y
- Index sensor ass'y
- Control PC board ass'y
- Clamp base plate aas'y
- Clamper ass'y

(1) Measuring instruments and tools
① Two channel oscilloscope
② Alignment disk
③ FDD tester
④ Phillips screwdriver for M2.5
⑤ Screw lock adhesive

(2) Check procedure
1. Connect the CH1 and CH2 terminals of the two channel oscilloscope to TP6 (index sensor output) and TP1 or TP2 (pre-amp output) on the control PC board respectively.
Setting of oscilloscope:
CH1: DC 2 V/div., 50 μsec/div.
CH2: AC 0.1 V/div., 50 μsec/div.
Trigger: CH1 at (+) trigger setting
2. Rotate the DD motor and load the alignment disk. It is assumed that the tracking alignment has been adjusted correctly in item 3-9.
3. Set the head to track 16.
4. Measure "t" as shown in Fig. 308.

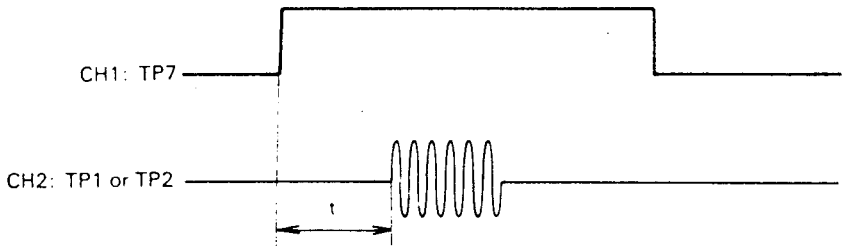


Fig. 308

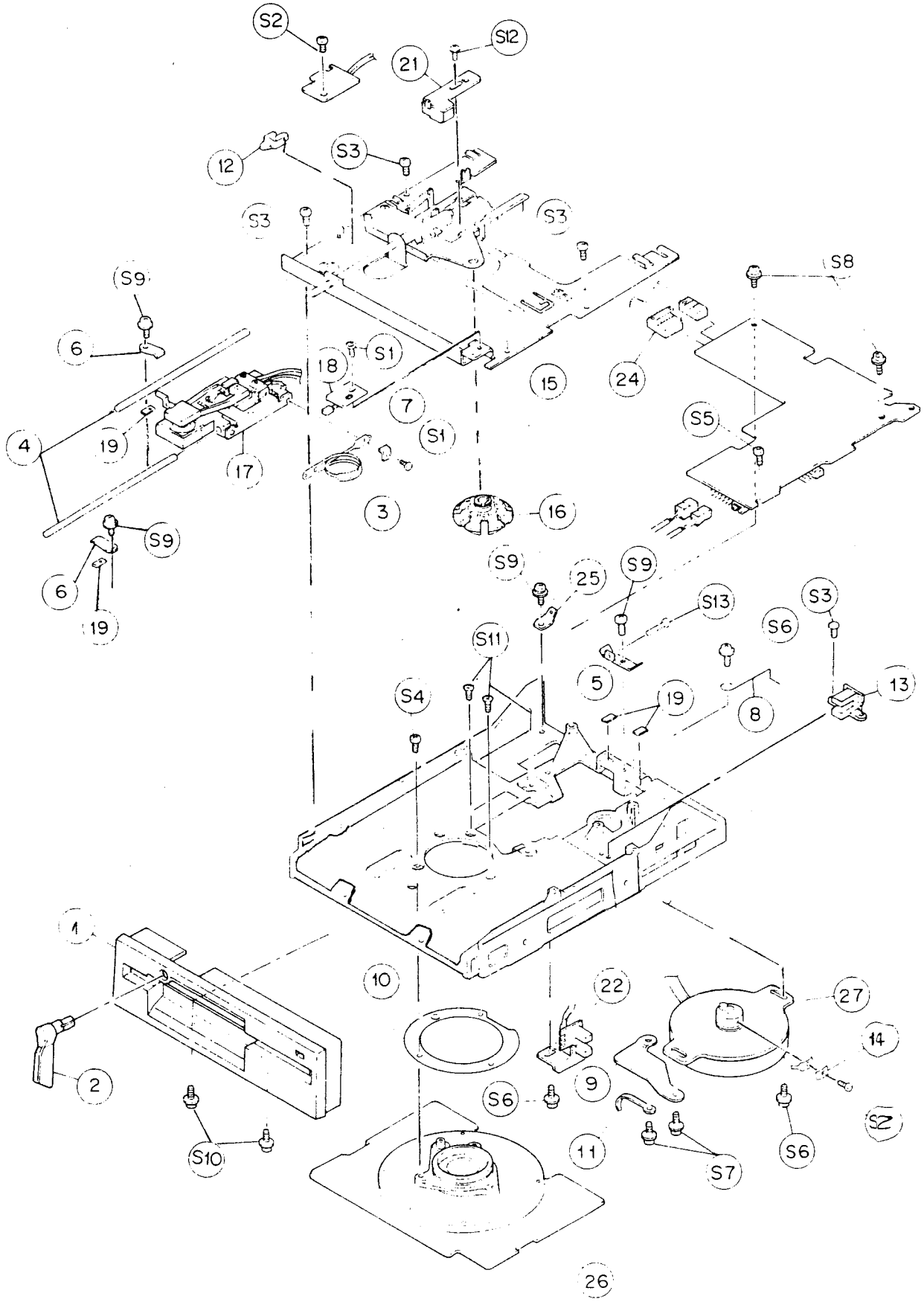
5. Check that value of the index burst timing "t" is within the range shown below. If outside the range, adjust in accordance with the adjustment procedure.
Index burst timing"t" = 200μsec ±200μsec

(3) Adjustment procedure
1. Loosen the mounting screw of the index sensor, then adjust the position of the index sensor so that the value of the index burst timing is within the specified range in step 5 in "Check". See Figs. 408 ~ 410.
2. Tighten the mounting screw to the specified torque, and execute steps 3 ~ 5 in "Check".
3. Apply a small amount of screw lock adhesive to the head of the mounting screw.
4. Check by TP7 that the output voltage of the index sensor is normal. (No waveform split should occur at "High" level of more than 3.0 V or at "Low" level of less than 0.5 V.)
5. Remove the alignment disk.
Note: In this check and adjustment, take care not to allow string external light to strike the index sensor.

Mechanism Parts List and Exploded View of F-502LII

NO.	PARTS NO.	DESCRIPTION	QTY	REMARKS
1		FRONT PANEL (BLACK)	1	
1		FRONT PANEL (BEIGE)	1	
2		FRONT LEVER (BLACK)	1	
2		FRONT LEVER (BEIGE)	1	
3		STEEL BELT	1	
4		RAIL	2	
5		RAIL RETAINER A	1	
6		RAIL RETAINER B	2	
7		STEEL BELT RETAINER	1	
8		SHIELD WIRE HOLDER	1	
9		SHIELD PLATE D	1	
10		P-ADJUSTMENT PLATE	1	ADJ. PARTS
11		WIRE HOLDER	1	
12		WP SOCKET	1	
13		DISK-IN SENSOR ASS'Y	1	
14		PULLEY WASHER	1	
15		CLAMP BASE PLATE ASS'Y	1	
16		CLAMPER ASS'Y	1	
17		HEAD CARRIAGE ASS'Y	1	
18		FRONT LED ASS'Y	1	
19		P-WASHER	4	ADJ.PARTS
20		W/P SENSOR ASS'Y	1	
21		INDEX SENSOR ASS'Y	1	
22		TRACK 00 SENSOR ASS'Y	1	
23		CONTROL PCB ASS'Y	1	
24		8 PIN CONNECTOR HOUSING	1	
25		FASTEN TERMINAL	1	
26		DD MOTOR ASS'Y	1	
27		STEPPING MOTOR ASS'Y	1	
S-1		SCREW 2 × 3	2	
S-2		SCREW 2.5 × 3	2	
S-3		SCREW 2.5 × 5	4	
S-4		SCREW 3 × 5	1	
S-5		SCREW 3 × 6	1	
S-6		SCREW 3 × 6 × 8 WS	3	
S-7		SCREW 3 × 8 × 8 WS	2	
S-8		SCREW 3 × 6 S	2	
S-9		SCREW 3 × 6 S	4	
S-10		SCREW 3 × 8 × 8 S	2	
S-11		SCREW 3 × 6	2	
S-12		SCREW 2 × 8 × 5 S	1	
S-13		SCREW 2 × 7	1	

Mechanism Exploded View of F-502LII



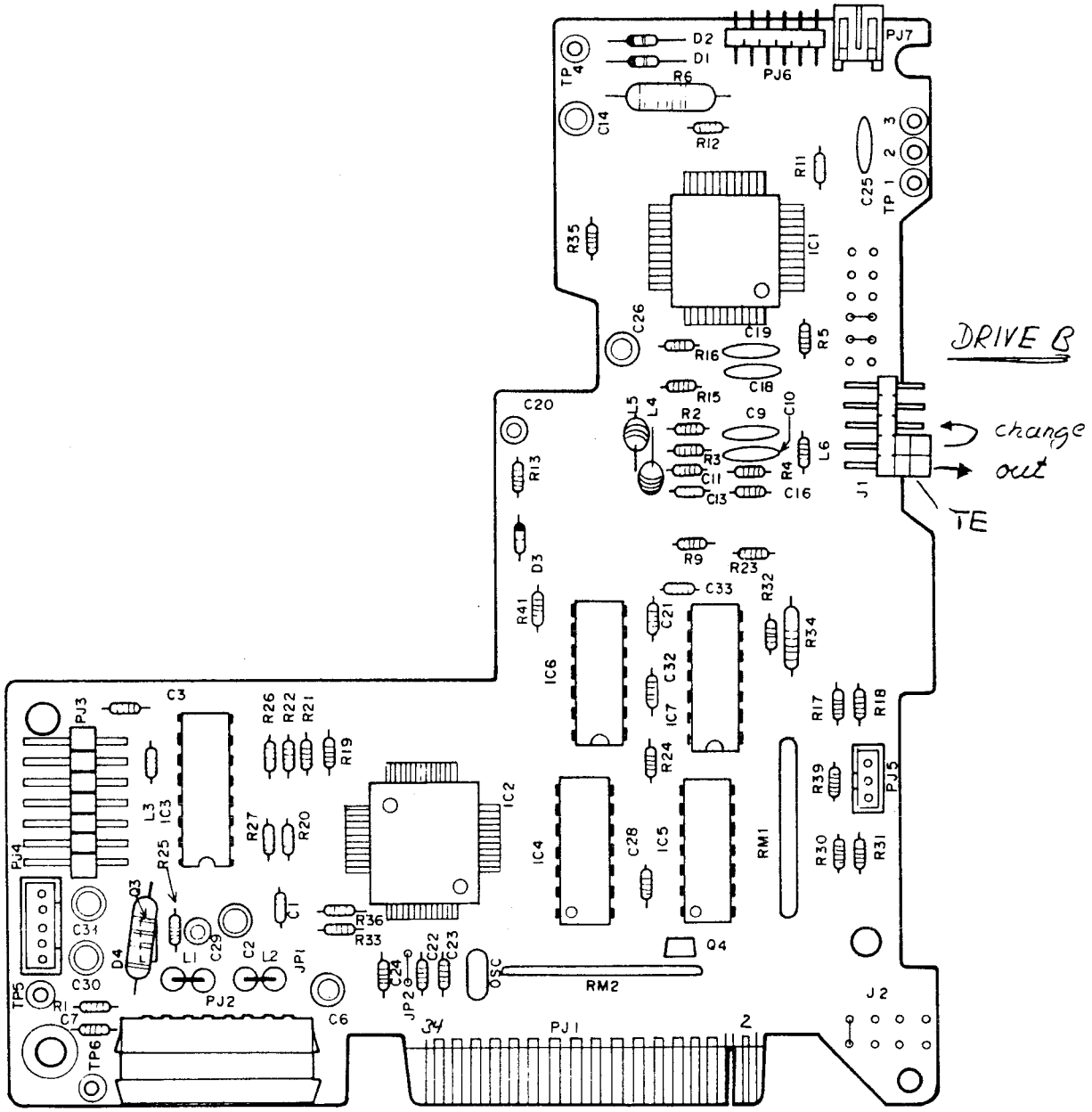
Electronical Parts List of Control PC Board Ass'y

The components of the control PC board ass'y are listed below.

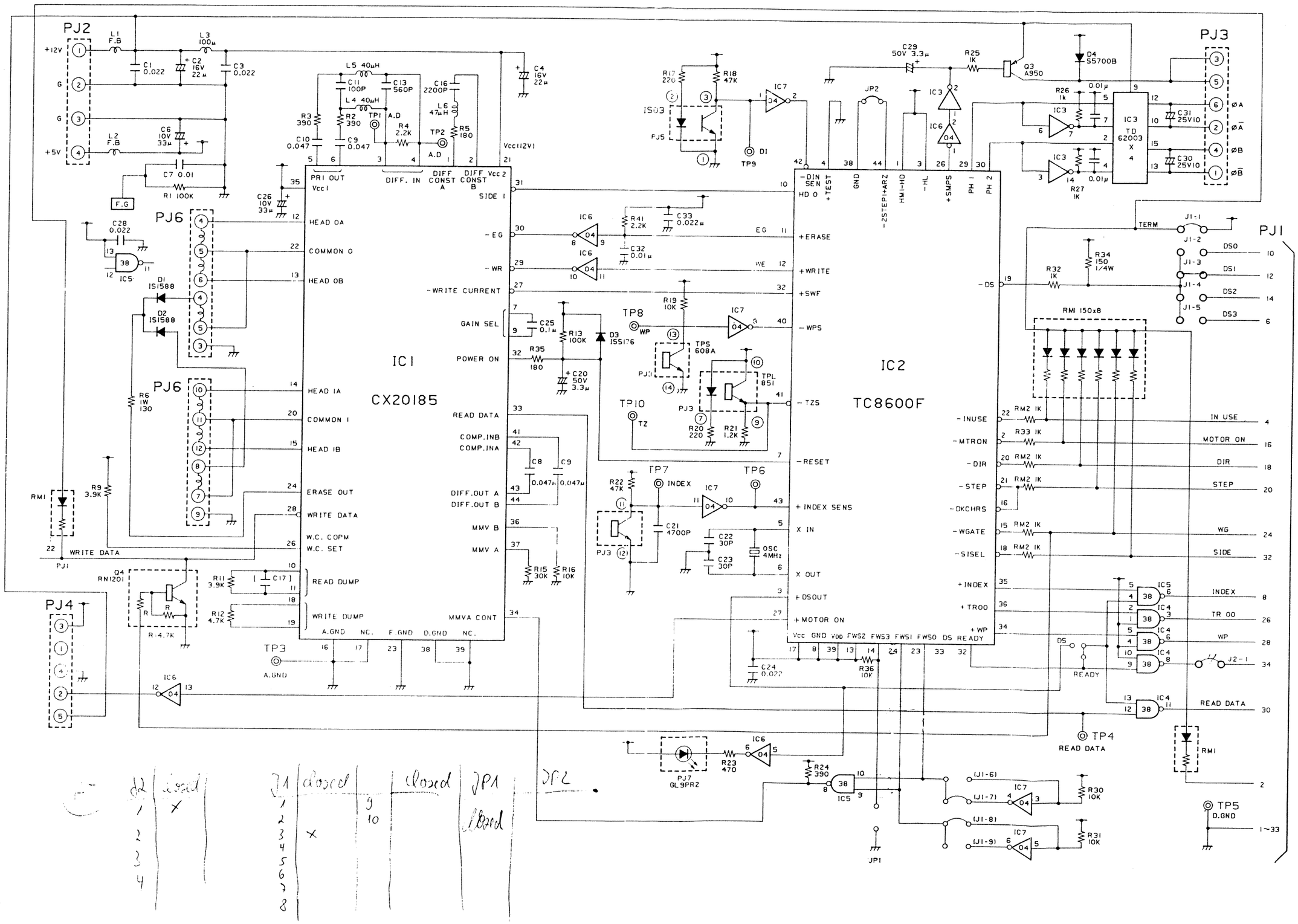
PARTS NO.	DESCRIPTION	QTY	REMARKS
	R/W IC. CX20185	1	IC1
	IC. TC8600SF	1	IC2
	IC. TD62003P	1	IC3
	IC. 7438	2	IC4, 5
	IC. 74LS04	2	IC6, 7
	TR. 2SA950	1	Q3
	TR. RN1201	1	Q4
	DIODE 1S1588	2	D1, 2
	DIODE 1SS176	1	D3
	DIODE S5566B	1	D4
	F-INDUCTOR BL02RN2-R62	2	L1, 2
	INDUCTOR 100μH	1	L3
	INDUCTOR 470μH	2	L4, 5
	INDUCTOR 47μH	1	L6
	CAPACITOR 560PF/50V	1	C13
	CAPACITOR 30PF/50V	2	C22, 23
	CAPACITOR 0.022μF/25V	5	C1, 3, 24, 28, 33
	CAPACITOR 100PF/50V	1	C11
	CAPACITOR 4700PF/16V	1	C21
	CERAMIC RESONATOR 4MHZ	1	OSC
	CAPACITOR 0.1μF/25V	1	C25
	CAPACITOR 0.047μF/16V	4	C9, 10, 18, 19
	CAPACITOR 0.01μF/16V	2	C7, 32
	CAPACITOR 2200PF/16V	1	C16
	CAPACITOR 22μF/16V	2	C2, 14
	CAPACITOR 33μF/10V	2	C6, 26
	CAPACITOR 3.3μF/50V	2	C20, 29
	CAPACITOR 10μ/25V	2	C30, 31
	RESISTOR 1/6W 180Ω	2	R5, 35
	RESISTOR 1/6W 220Ω	2	R17, 20
	RESISTOR 1/6W 390Ω	3	R2, 3, 24

PARTS NO.	DESCRIPTION	QTY	REMARKS
	RESISTOR 1/6W 470Ω	1	R23
	RESISTOR 1/6W 1KΩ	5	R25, 26, 27, 32, 33
	RESISTOR 1/6W 1.2KΩ	1	R21
	RESISTOR 1/6W 2.2KΩ	2	R4, 41
	RESISTOR 1/6W 3.9KΩ	2	R9, 11
	RESISTOR 1/6W 4.7KΩ	1	R12
	RESISTOR 1/6W 10KΩ	6	R16, 19, 30, 31, 36, 39
	RESISTOR 1/6W 30KΩ	1	R15
	RESISTOR 1/6W 47KΩ	2	R18, 22
	RESISTOR 1/6W 100KΩ	2	R1, 13
	RESISTOR 1W 130Ω	1	R6
	RESISTOR 1/4W 150Ω	1	R34
	R-PACK 150Ω X 8 1/8W	1	RM1
	R-PACK 1KΩ X 5 1/8W	1	RM2
	SHORT PLUG	2	J1
	SHORT PIN 10PIN	1	J1
	JUMPER WIRE	3	J1, J2
	JUMPER WIRE	1	JP2
	POWER CONNECTOR 4PIN	1	PJ2
	BAND	1	PJ2
	2PIN CONNECTOR MALE (LED)	1	PJ7
	4PIN CONNECTOR (DD MOTOR)	1	PJ4
	3PIN CONNECTOR (DISK-IN)	1	PJ5
	12PIN CONNECTOR (HEAD)	1	PJ6
	14PIN CONNECTOR (SENSOR)	1	PJ3

Location of Electronical Parts



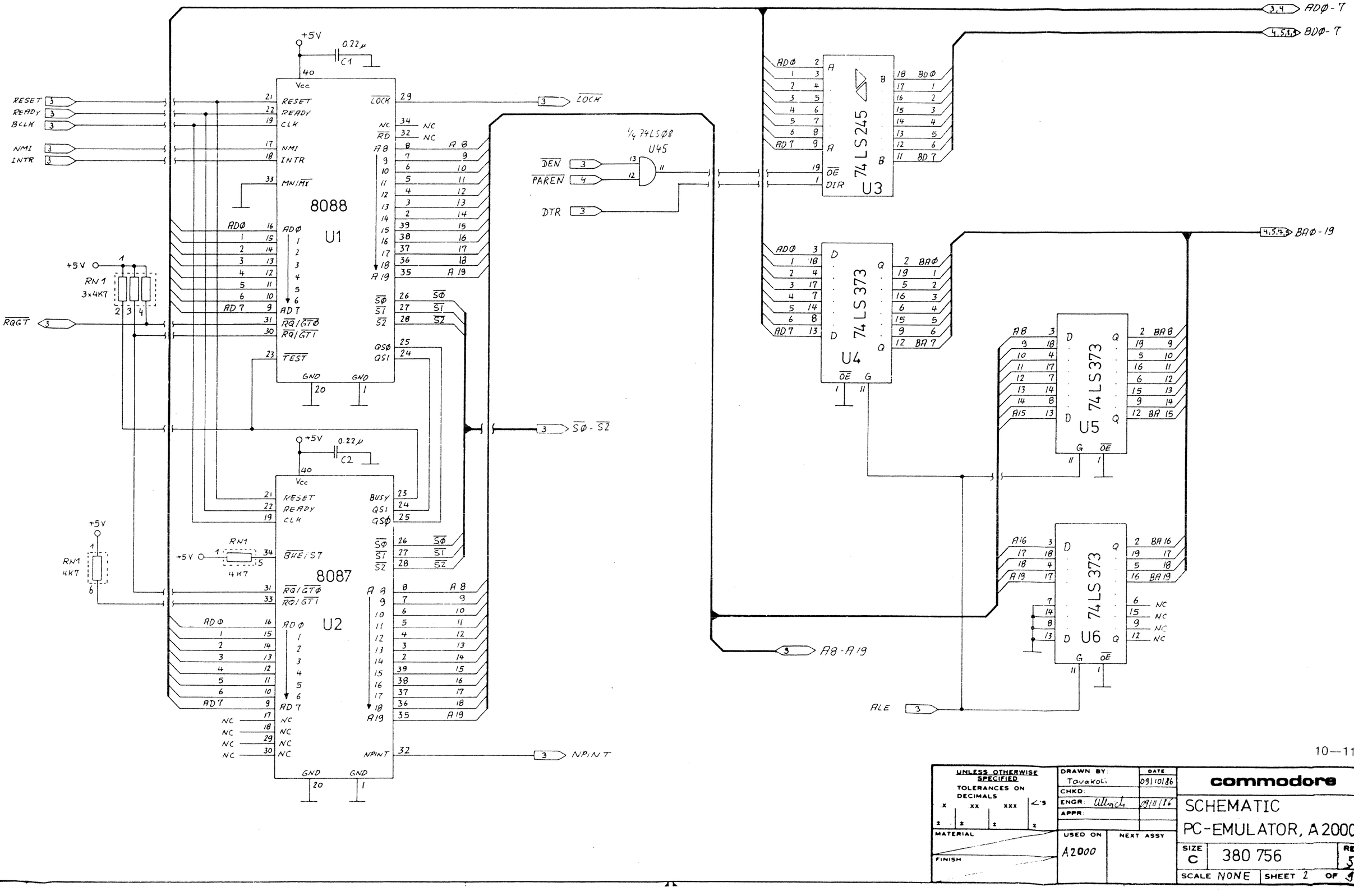
5-6. Schematic Diagram for F-502II/F-502LII



J2	Used
1	×
2	
3	
4	

J1	closed		closed	JP1
1		9		Used
2		10		
3	×			
4				
5				
6				
7				
8				

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



10—11

UNLESS OTHERWISE SPECIFIED TOLERANCES ON DECIMALS .X ±, .XX ±, .XXX ±, ∠'S ±	DRAWN BY: Tavakoli	DATE: 09/10/86
	CHKD:	
	ENGR: [illegible]	29/11/86
	APPR:	
MATERIAL / FINISH	USED ON: A2000	NEXT ASSY:

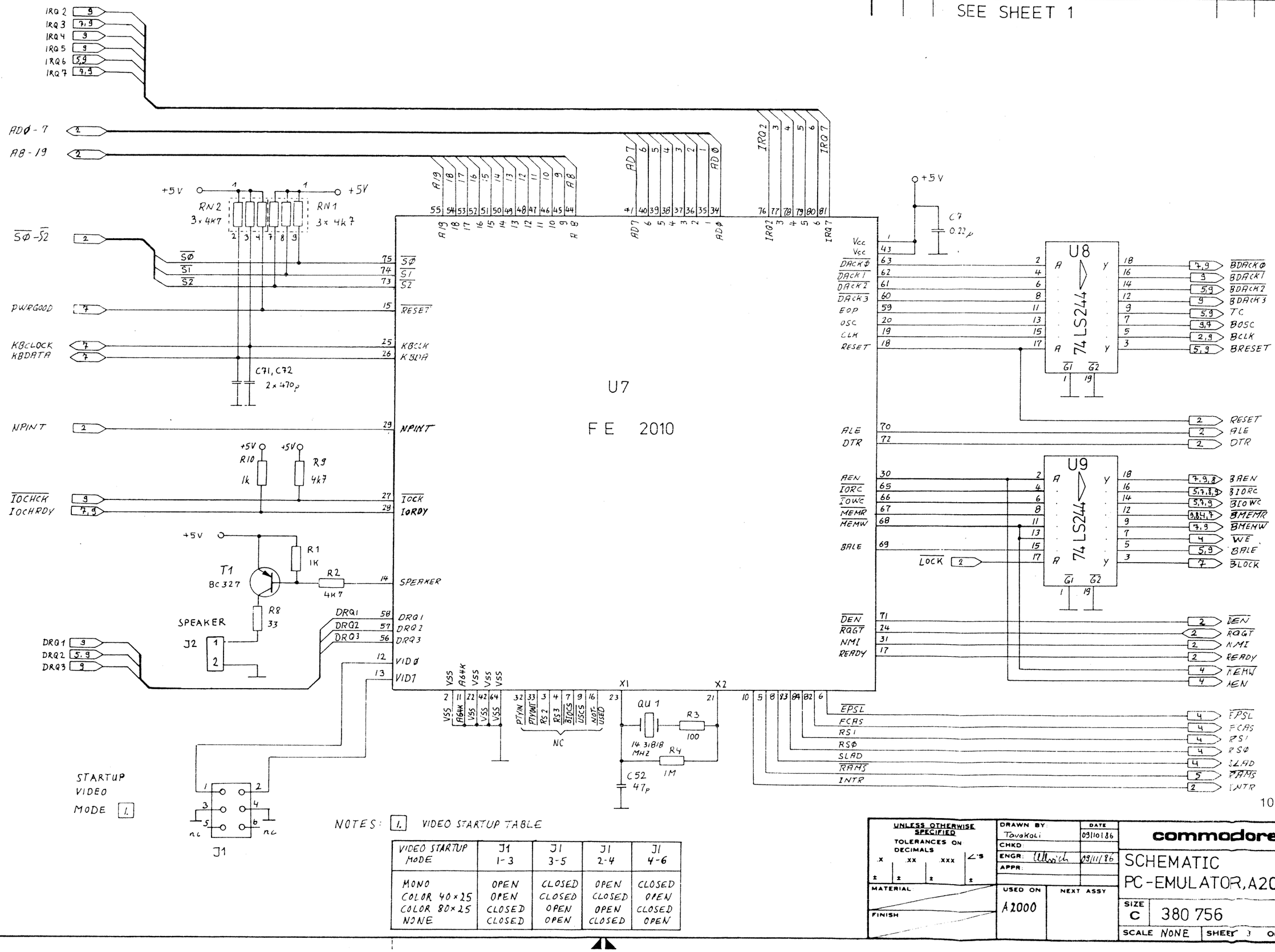
commodore

SCHEMATIC

PC-EMULATOR, A2000

SIZE		REV
C	380 756	5
SCALE NONE	SHEET 2 OF 9	

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



NOTES: [1.] VIDEO STARTUP TABLE

VIDEO STARTUP MODE	J1 1-3	J1 3-5	J1 2-4	J1 4-6
MONO	OPEN	CLOSED	OPEN	CLOSED
COLOR 40×25	OPEN	CLOSED	CLOSED	OPEN
COLOR 80×25	CLOSED	OPEN	OPEN	CLOSED
NONE	CLOSED	OPEN	CLOSED	OPEN

UNLESS OTHERWISE SPECIFIED TOLERANCES ON DECIMALS .X ±, .XX ±, .XXX ±, ∠ ±°	DRAWN BY: TavaKoLi	DATE: 09/10/86
	CHKD:	
	ENGR: Ulrich	09/11/86
	APPR:	
MATERIAL / FINISH	USED ON: A2000	NEXT ASSY

commodore

SCHEMATIC
PC-EMULATOR, A2000

SIZE		REV
C	380 756	5
SCALE NONE	SHEET 3 OF 9	

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

BA 0-19

74 HCT 158 U10 (B/Ā)

74 HCT 158 U11 (SEL B/Ā)

RN3 4×68 — MRA0 MRA1 MRA2 MRA3

RN4 4×68 — MRA4 MRA5 MRA6 MRA7

RN5 4×68 — MRA8

R5 100

WE 3

SLAD 3

BANK 0: U12 U13 U14 U15 U16 U17 U18 U19

BANK 1: U20 U21 U22 U23 U24 U25 U26 U27

+5V, 8 × 0µ22 C12-19

8 x DRAM 256K x 1

+5V, 8 × 0µ22 C20-C27

8 x DRAM 256K x 1

MRD7 MRD6 MRD5 MRD4 MRD3 MRD2 MRD1 MRD0

AMUX 8, MRAS 1, MRAS 0, MCAS

+5V C28 0µ22

27128/23128 U28

+5V C29 0µ22

PAL16L8 U29

RAM-DECODER

RS0 3, RS1 3, FCAS 3, A18AND19 5, EPSL 3

BA 14, 15, 16, BA 17

MEMW 2, AEN 2, PAREN 2, ROMEN

AD0-7 2

74 LS 245 U30

MRD7 MRD6 MRD5 MRD4 MRD3 MRD2 MRD1 MRD0

BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0

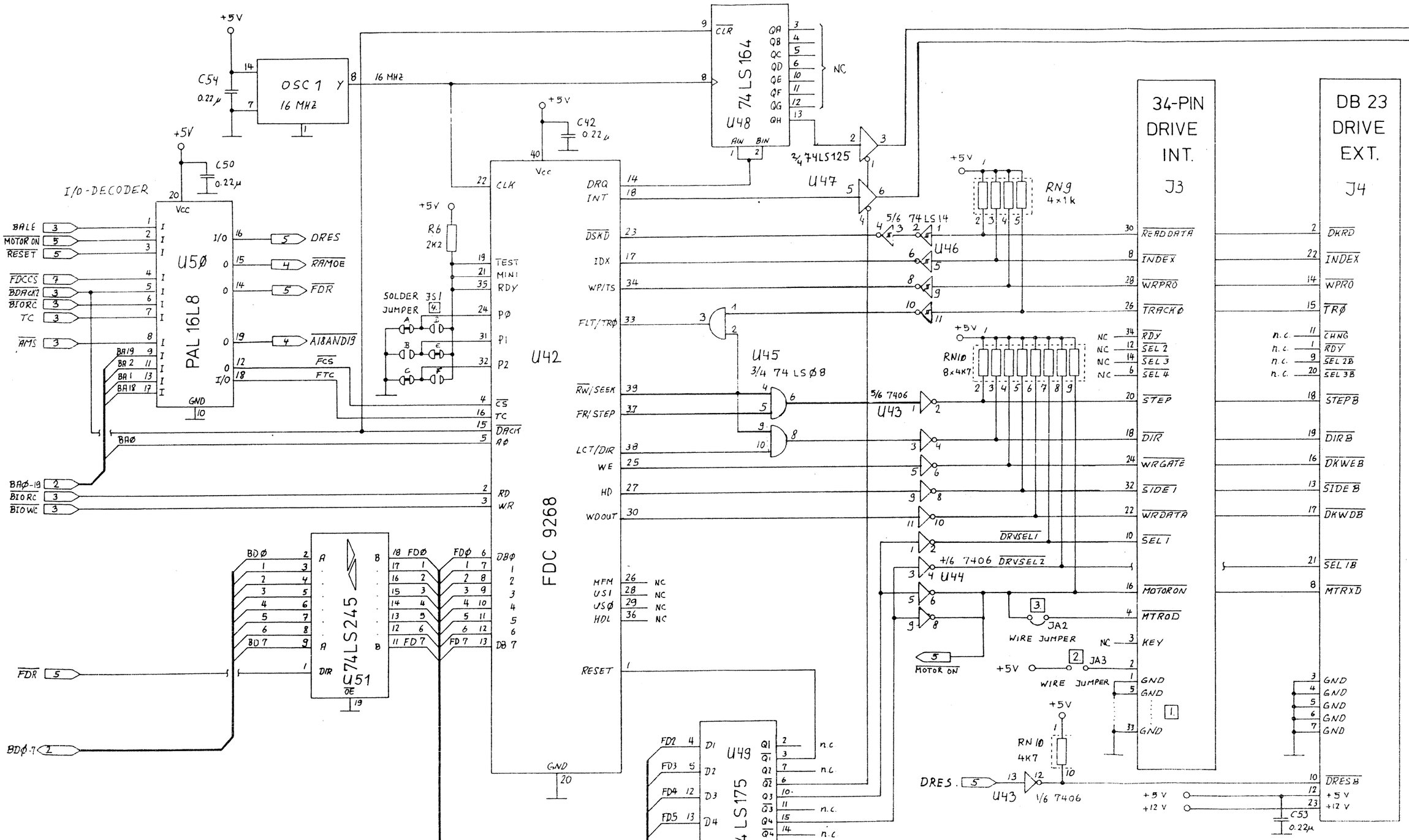
BD0-7 2

RAMOE 5, BMEMR 3

10—13

UNLESS OTHERWISE SPECIFIED TOLERANCES ON DECIMALS .X ± .XX ± .XXX ± ∠'S ±	DRAWN BY: Wanta	DATE 09/01/86	commodore
	CHKD:		SCHEMATIC
	ENGR: Ullrich	09/11/86	PC-EMULATOR, A 2000
	APPR:		
MATERIAL / FINISH	USED ON A 2000	NEXT ASSY	SIZE C 380 756 REV 5
			SCALE NONE SHEET 4 OF 9

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



NOTES:
1. ALL ODD PINS OF J3 CONNCTED TO GND
2. WIRE JUMPER NORMALY OPEN
3. WIRE JUMPER NORMALY CLOSED
4. FDC WRITE PRECOMP. SELECTION DEFAULT IS 250ns

UNLESS OTHERWISE SPECIFIED	DRAWN BY:	DATE
TOLERANCES ON DECIMALS .X ± .XX ± .XXX ± ∠'S ±	Tavakoli	09/10/86
	CHKD:	
	ENGR: Ulrich	09/11/86
	APPR:	
MATERIAL / FINISH	USED ON: A2000	NEXT ASSY

commodore

SCHEMATIC

PC-EMULATOR, A2000

SIZE		REV
C	380 756	5
SCALE NONE	SHEET 5 OF 9	

REVISIONS				Chapter 10
LTR	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

RAØ -7

MUXSEL

RAMEN

DELAY LINE U31 100ns — 50ns — IN — VCC — GND — +5V — C31 0µ22 — RN6 33 — CAS

2 DRAM 64K x 4 — U32 U33 — U34 U35

AØ A1 A2 A3 A4 A5 A6 A7 WE CAS VDD VSS G — RAØ RA1 RA2 RA3 RA4 RA5 RA6 RA7 WE CAS VDD VSS

+5V — C32 - C35 4x0.22µ — VDD VSS

RRASØ — 68 RN6 — RAS

D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D4 D2 D1 D0

RD15 RD14 RD13 RD12 RD11 RD10 RD9 RD8 RD7 RD6 RD5 RD4 RD3 RD2 RD1 RD0

RDØ-15

4x68 RN7 — AØ A1 A2 A3 — RAØ RA1 RA2 RA3

2x68 RN6 — WE RAS — RWE RRAS1 — 100p C55

4x68 RN8 — A4 A5 A6 A7 — RA4 RA5 RA6 RA7

74 HCT 257 U36 — 1B 2B 3B 4B 1A 2A 3A 4A — 1Y 2Y 3Y 4Y — SEL B/Ā OE — MA1 MA2 MA3 MA4 MA9 MA10 MA11 MA12

74 HCT 257 U37 — MA5 MA6 MA7 MA8 MA13 MA14 MA15 MA16

MUXSEL

A68KEN

MA1-23

MA4 MA5 MA6 MA7 MA8 MA9 MA10 MA11 MA12 MA13 MA14 MA15 MA16

74 LS 133 U38

MREG

CONFIGURATION

*) PAL16L8 U39 — RD12 RD13 RD14 RD15 — MA1 MA2 MA3 MA4 MA5 MA6 — N.C.

SHUT_UP PRE_CONFIG CONFIG_OUT

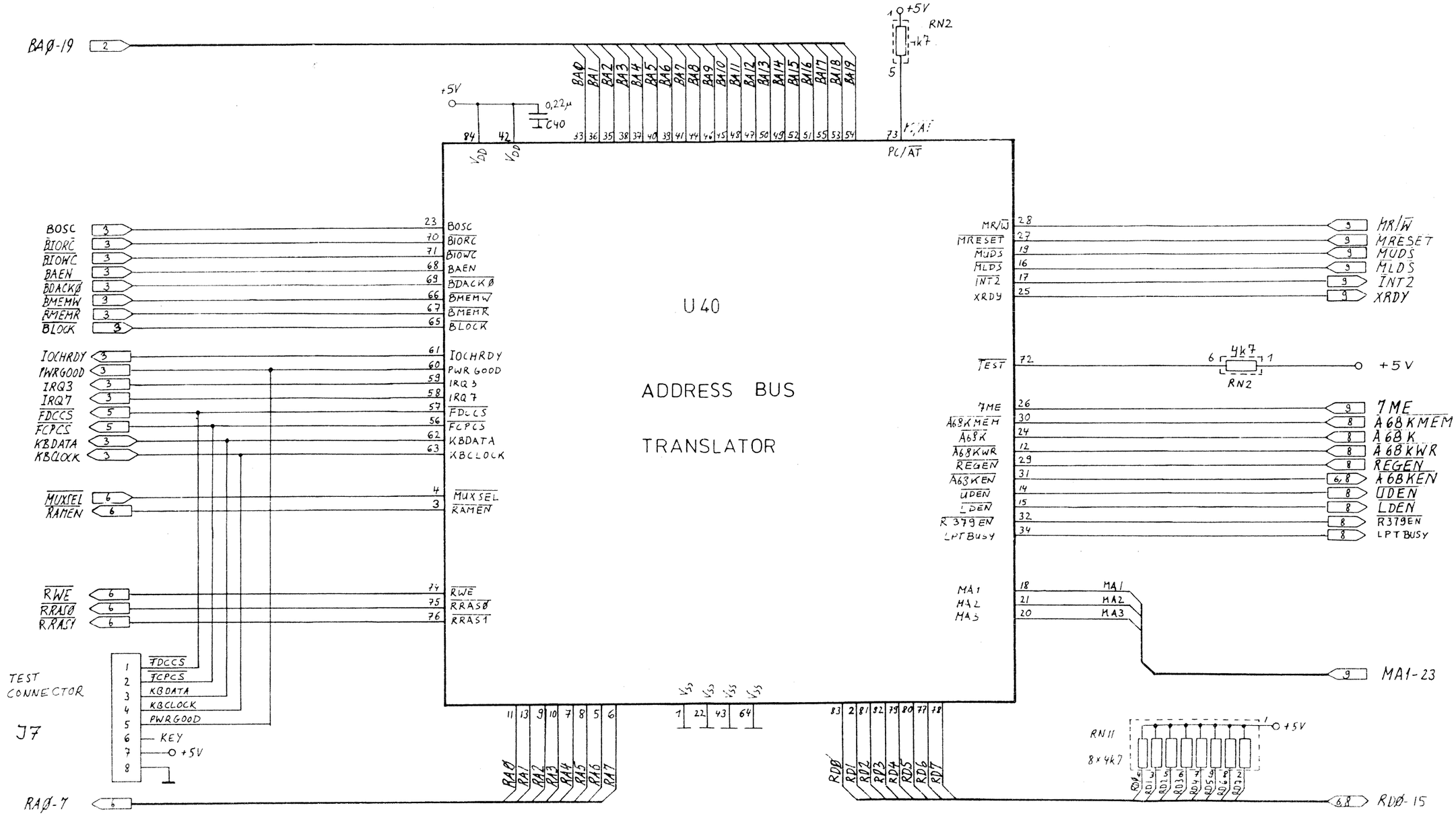
MKIW MRESET MUDS BOARD_SEL

*) EXT. PAL
ONLY USED IF CONFIG_EN
JUMPER OPEN (JA1)

10--15

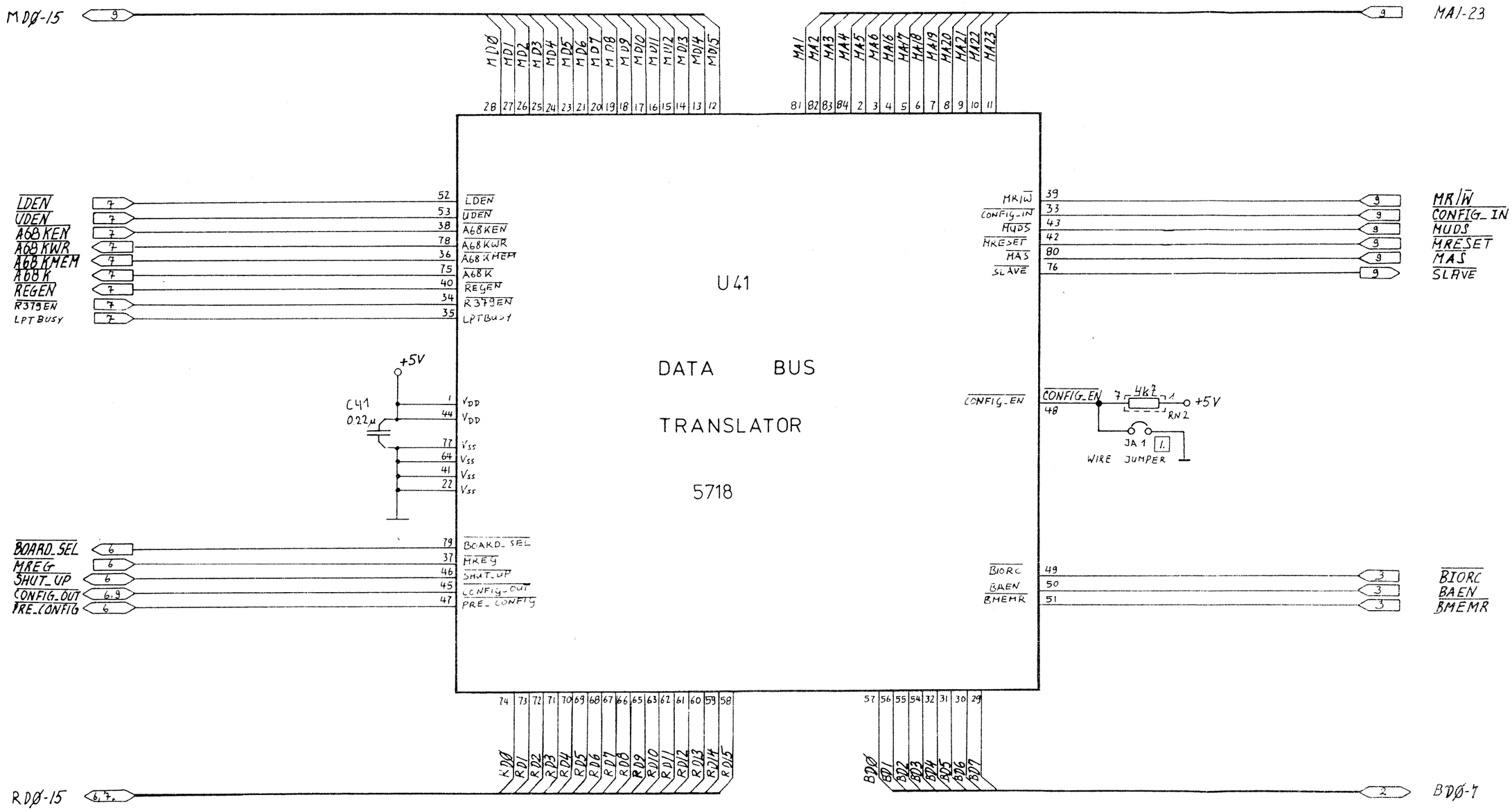
UNLESS OTHERWISE SPECIFIED TOLERANCES ON DECIMALS .X ± .XX ± .XXX ± ∠'S ±	DRAWN BY Warta	DATE 09/10/86	commodore
	CHKD		SCHEMATIC
	ENGR Ullrich	09/11/86	PC-EMULATOR, A2000
	APPR		
MATERIAL / FINISH	USED ON A2000	NEXT ASSY	SIZE C — 380 756 — REV 5
			SCALE NONE — SHEET 6 OF 9

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



UNLESS OTHERWISE SPECIFIED TOLERANCES ON DECIMALS X ± .XX ± .XXX ± ∠'S ±	DRAWN BY: Warta	DATE: 09/10/86	commodore
	CHKD:		SCHEMATIC
	ENGR: [illegible]	09/11/86	PC-EMULATOR, A2000
	APPR:		
MATERIAL / FINISH	USED ON: A2000	NEXT ASSY	SIZE C · 380 756 · REV 5
			SCALE NONE · SHEET 7 OF 9

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



NOTES: [4] WIRE JUMPER NORMALLY CLOSED. IF CLOSED, CONFIG PAL INTERNALLY OF U41 IS USED. U39 MUST NOT BE INSERTED IN THIS CASE.

UNLESS OTHERWISE SPECIFIED TOLERANCES ON DECIMALS .X ± .XX ± .XXX ± ∠'S ±	DRAWN BY: Warta	DATE 09/10/86	commodore
	CHKD:		SCHEMATIC
	ENGR: Ulrich	09/11/86	PC-EMULATOR, A 2000
	APPR:		
MATERIAL / FINISH	USED ON A2000	NEXT ASSY	SIZE C 380 756 REV 5
			SCALE NONE SHEET 8 OF 9

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

CARD EDGE
100 pol.

J5

MA 1-23 (6,8,7)

MA 1	29
MA 2	27
MA 3	26
MA 4	24
MA 5	21
MA 6	23
MA 7	28
MA 8	30
MA 9	32
MA 10	34
MA 11	36
MA 12	38
MA 13	39
MA 14	41
MA 15	43
MA 16	45
MA 17	47
MA 18	52
MA 19	54
MA 20	56
MA 21	58
MA 22	57
MA 23	59

MD 0-15 (8)

MD 0	75
MD 1	77
MD 2	79
MD 3	81
MD 4	83
MD 5	86
MD 6	84
MD 7	82
MD 8	80
MD 9	78
MD 10	76
MD 11	71
MD 12	69
MD 13	67
MD 14	65
MD 15	63

19	7 INT 2
18	7 XRDY
12	8 CONFIG_IN
11	6,8 CONFIG_OUT
9	8 SLAVE
84	7,8,6 MRESET
69	7,8,6 MR/W
74	8 MAS
70	7 MLDS
72	7,8,6 MUDS
92	4 7ME
1-4, 13, 25, 37, 49, 61, 73, 85, 87-91, 99, 100	
5, 6	+5V
7, 8, 10, 14-17, 20-22, 31, 33, 35, 40, 42, 44, 46, 48, 50, 51, 53, 55, 60, 62, 64, 66, 93, 95, 96, 97, 98	n.c.

+5V → +5V
3 x 47µ/16V C56-58
1 x 0.22µ C39
20 x 0.1µ C3-6, C8-C11, C30, C36, C37-38, C43-49, C51

+12V → +12V
1 x 47µ/25V C59
1 x 0.22µ C60

SPARE:

U47 2/4 74LS125 U44 2/6 7406

+5V
R11 1k
NC
NC

CARD EDGE
2 x 31 pol.

J6

B		A	
B01		A01	3 IOCHCK
B02	BRESET (3)	A02	BD 7
B03	0.22µ C70 +5V	A03	6
B04	IRQ 2 (3) 100p C61 nc	A04	5
B05		A05	4
B06	DRQ 2 (3) C62 nc	A06	3
B07	nc	A07	2
B08	nc	A08	1
B09	+12V	A09	BD 0
B10		A10	3 IOCHRDY
B11	BMEMW (3)	A11	3 BAEN
B12	BMEMR (3)	A12	BA 19
B13	BIOWC (3)	A13	18
B14	BIORC (3)	A14	17
B15	BDACK3 (3)	A15	16
B16	DRQ3 (3) 100p C63	A16	15
B17	BDACK1 (3)	A17	14
B18	DRQ 1 (3) 100p C64	A18	13
B19	BDACK0 (3)	A19	12
B20	BCLK (3)	A20	11
B21	IRQ 7 (3) 100p C65	A21	10
B22	IRQ 6 (3) 100p C66	A22	9
B23	IRQ 5 (3) 100p C67	A23	8
B24	IRQ 4 (3) 100p C68	A24	7
B25	IRQ 3 (3) 100p C69	A25	6
B26	BDACK2 (3)	A26	5
B27	TC (3)	A27	4
B28	BALE (3)	A28	3
B29	+5V	A29	2
B30	BOSC (3) R7 33	A30	1
B31		A31	BA 0

2 BA 0-19

UNLESS OTHERWISE SPECIFIED TOLERANCES ON DECIMALS .X ± .XX ± .XXX ± ∠'S ±
MATERIAL:
FINISH:

		DATE
DRAWN BY:	Warta	08/08/86
CHKD:		
ENGR:	Ulrich	09/10/86
APPR:		

USED ON: A2000
NEXT ASSY:

commodore

SCHEMATIC
PC-EMULATOR, A 2000

SIZE C | 380 756 | REV 5
SCALE NONE | SHEET 9 OF 9